Monte Carlo Simulations to Evaluate the Contribution of Si Bulk, Interconnects, and Packaging to Alpha-Soft Error Rates in Advanced Technologies

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***Abstract*—At ground level, alpha particles are a major source of soft errors. They may result from radioactive isotopes found in electronic device materials. In this paper, the materials' contributions to alpha particle-induced Soft Error Rate (SER) and MCU are evaluated for a 65 nm CMOS technology. The trend of SER on 45 and 32 nm is also reported in this paper. These evaluations are performed by Monte Carlo simulations, taking into account the radioactive impurity contamination levels in the device.**

***Index Terms*—Alpha particles, bulk, interconnects, MC-ORACLE, packaging, soft errors.**

I. Introduction

With the continuous technology downscaling, Complementary Metal Oxide Semiconductor (CMOS) devices become more sensitive to soft errors. This sensitivity (to soft errors) is increasing with decreasing device dimensions and operating voltage in recent technologies. An important parameter is the critical charge, which is the minimum amount of charge required to change a stored data bit from the state "1" to the state "0" or *vice versa*. There are two primary radiation sources causing soft errors at ground level: atmospheric neutrons and alpha particles. Atmospheric neutrons indirectly generate charges by colliding with nuclei within the chip materials. The products of such collisions are secondary ions capable of creating soft errors [1]–[4]. On the other hand, alpha particles directly generate charges by losing their energy and ionizing atoms of the medium in which they travel, resulting in charge generation, which may then be collected by sensitive nodes [5]. A recent study [6] showed the contribution to the Soft Error Rate (SER) by alpha particles at ground level is twice as great as that of neutrons for a 65 nm technology, even with high purity package materials with an alpha emission rate of $9 \times 10^{-4}\ \alpha/\mathrm{cm}^2\ \mathrm{hr}$. This shows the importance of alpha particles to soft errors compared to atmospheric neutrons. In previous work [7], the contribution of the silicon bulk to SER due to alpha particles has been evaluated, but the SER contributions of different parts of an electronic device were not evaluated. The aim of this paper is to evaluate and compare the SER contribution of the Si bulk, interconnect systems, and flip chip package materials. In order to compare their contributions to the SER, a simplified model of a 65 nm technology is simulated with a Monte Carlo energy-deposition tool, taking into account the alpha emission rate (AER).

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II. Sources of Alpha Particles

Alpha particles result from natural decay of some radioactive isotopes. An exhaustive list of all alpha emitting isotopes that may create soft errors has been studied in [8]. In electronic devices, there are two types of alpha-emitting isotopes. The first ones are natural radioactive impurities occurring naturally in the materials used to fabricate electronic devices. As downscaling continues, the semiconductor industry needs new chemical elements to overcome scaling issues. However, among these newly added chemical elements in devices some have alpha emitting isotopes (e.g., hafnium [9]). A recent work [10] has studied the contributions of these new elements to the SER. The second ones are naturally incorporated in trace amounts as impurities in some materials used to manufacture chips or result from process-related factors, such as residuals left behind from etching (e.g., phosphoric acid). The common radioactive impurities in integrated circuits (ICs) are $^{238}\mathrm{U}$, $^{232}\mathrm{Th}$ [1]–[5]s and their descendants' nuclei. $^{238}\mathrm{U}$ and $^{232}\mathrm{Th}$ are mother nuclei of eight and seven alpha-emitting isotopes, respectively. This paper deals with contamination from radioactive impurities. All materials or parts of devices' containing radioactive impurities do not participate in inducing soft errors because of the distance separating them from the sensitive volumes. If the contaminated parts of an IC are far from sensitive volumes, the probability of alpha particles emitted by these zones to reach sensitive volumes decreases. Thus, it is important to know and study materials surrounding sensitive volumes to determine which part of electronic devices contribute to soft errors.

A. Simplified Structure of an IC With Flip-Chip Assembly

The semiconductor industry has moved toward the ball grid array (BGA) to support high lead count packages and among BGA packaging, the flip chip BGA has been well accepted as an important vehicle [11]. In this paper, we consider flip chip packaging. A flip chip packaging approach offers the following advantages: area array packaging, electrical performance, low-

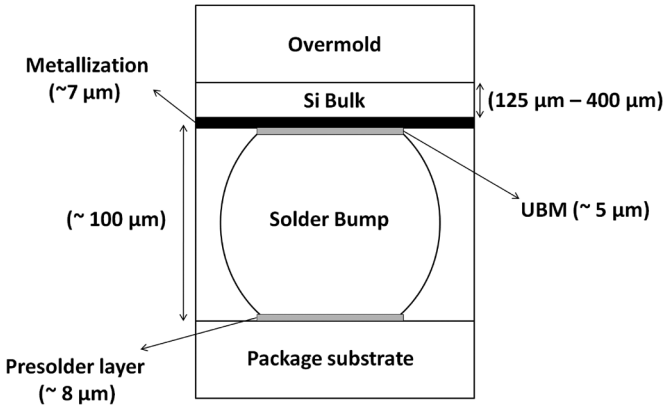

Fig. 1. Cross-sectional views of simplified flip chip device. (Not to scale).

cost assembly, and reliability [12]. Fig. 1 is a simplified cross-sectional view of an IC using the flip chip attachment and its main characteristics are represented. The Under Bump Metallurgy (UBM) or Ball Limiting Metallurgy (BLM) is a layer protecting the IC final metal from the environment and the solder bump is a ball like structure that provides the contact between the chip package and the printed circuit board (PCB). Furthermore, the flip chip attachment uses underfill protecting the underside of the device from the environment. It also increases the reliability by increasing fatigue life and by reducing the temperature of the IC [12]. Finally, in order to complete the packaging process of a flip chip, a presolder layer and a package substrate is required to link the solder bump to the PCB. Generally in flip chips, the package substrate is a layer allowing the connections of solders bumps to the next levels of packaging in which substrate vias are found. For flip chips, it is made of a rigid laminate [12]. Moreover, an overmold compound surrounds the Si bulk in order to protect it from the external environment. The Si bulk thickness depends on the application and its minimum value is around 125 μm [13]. Typical dimensions of the different materials are represented in Fig. 1.

As the sensitive volumes are located in the Si bulk near the interface between the Si bulk and the metallization layer, this paper focuses on the materials surrounding this interface. According to Fig. 1, the materials surrounding the surface are the Si bulk, interconnects, Under Bump Metallization (UBM), underfill, solder bump, presolder layer and the package substrate. In this paper, a solder bump made of an alloy (Pb37Sn63) [12] is considered. The Si bulk, interconnects system, UBM, under fill are represented by Si, SiO_2, Cu, and epoxy, respectively. Once the materials are selected, the next step is to determine if alpha particles emitted by these materials (in case of contamination) can reach the surface of the Si bulk.

B. Range of Alpha Particles in Materials Surrounding the Die

^{238}U, ^{232}Th and their relative daughter nuclei are the main alpha contaminants. The energy of alpha particles emitted by these nuclei is between 4 and 9 MeV [3]. Using SRIM [14], the maximum range of alpha particles in electronic materials is reported in Table I. According to Table I, in the worst case, alpha particles travel 60 μm before stopping. Therefore, an alpha particle should be emitted, in the worst case, within 60 μm of the sensitive region of the Si bulk surface to cause a soft error. From Fig. 1, the areas of ICs which are within 60 μm of the surface are the Si bulk, UBM, under fill, and solder bump. Alpha particles emitted from the presolder layer found around 100 μm from the bulk surface (see Fig. 1) cannot reach the sensitive volumes and are not able to induce soft errors.

However, a presolder layer with a high level of radioactive (UA level see Section III-A) contamination can induce soft errors by diffusion of its radioactive impurities to the surface of the die during processing [15]. In this paper, by assuming that the 65 nm technology has a presolder layer having a Ultra Low Alpha (ULA), diffusion of radioactive impurities to the Si surface is not considered. As the minimum thickness of the Si Bulk is around 125 μm and the maximum range of alpha is around 60 μm, the overmold compound surrounding the Si bulk does not contribute to SER. Once the critical zone inducing soft errors is determined, the quantity of radioactive impurities of the materials found in this critical zone is evaluated in the next section in order to estimate their contributions to soft errors.

TABLE I
MAXIMUM RANGE OF ALPHA PARTICLES IN DIFFERENT MATERIAL USED IN IC'S PROCESS CALCULATED WITH SRIM

Material	Maximum range of alpha particle (µm) (alpha particle energy 9 MeV)
Si	59.05
SiO_2	53.25
Cu	22.88
Epoxy	50.75
Solder Bump (Pb37Sn63)	34.56

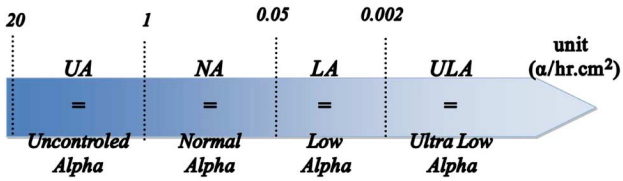

Fig. 2. Material classification according to the alpha emission rate.

III. RADIOACTIVE IMPURITIES LEVEL IN CRITICAL MATERIALS

A. Alpha Emission Rate (AER)-Based Classification

The alpha emission rate (AER) is a method to count the alpha particles escaping from an area in a given period of time. It allows determination of the purity grade of a given material. Based on their AER, materials are classified into four categories, Uncontrolled Alpha (UA), Normal Alpha (NA), Low Alpha (LA), Ultra Low Alpha (ULA) (see Fig. 2) [16]. Table II represents the AER of different materials used for the chip substrate, interconnects, and for flip chip packaging, according to JEDEC standard (JESD89A) [17].

In 2008, the AER requirement was $0.001\alpha/\mathrm{cm}^2 - \mathrm{hr}$ [18]. The materials presented in Table II satisfy this specification, except underfills and solder bumps. According to Table II, underfills cover two categories, the LA and ULA. The case of solder

TABLE II
EQUIVALENT URANIUM CONCENTRATION OF ALPHA EMISSION RATE

Material	AER [17] (α/cm^2/hr)	Equivalent ^{238}U concentration calculated with MC-ORACLE
Fully Processed Wafers (bulk)	<0.0004	< 120 ppt
30 µm thick Cu	<0.0003	< 220 ppt
Flip Chip Underfill	0.0007< - <0.004	150 ppt< - <855 ppt
Pb based Solder Bump (Packaging)	0.0009< - <7.2	0.44 ppb< - <3523 ppb

bumps is critical. Their AERs cover almost the entire range of the radioactive contamination categories. This makes solder bumps the most crucial materials triggering alpha particle-induced soft errors. Using the AERs of these materials, the equivalent radioactive impurity of $^{238}\mathrm{U}$ contents are calculated by using a Monte Carlo simulation tool called MC-ORACLE. In this paper, we considered only $^{238}\mathrm{U}$ because at secular equilibrium the $^{238}\mathrm{U}$ decay chain has an AER which is four times greater than $^{232}\mathrm{Th}$ decay chain.

B. MC-ORACLE: A Monte Carlo Tool

MC-ORACLE is a predictive tool for SER, as well as for SEU and MCU cross sections based on the Monte Carlo Method due to protons, neutrons, and alpha particles [19]. This code also permits evaluating the contamination level of different material to be estimated based on their AER (see Section III-C). When traveling different materials, the energy loss of alpha particles in these materials is evaluated with SRIM.

C. Simulation and Results

Some assumptions are made in order to evaluate the corresponding quantity of radioactive impurities of the AERs mentioned in Table II. The assumptions are the following. The radioactive impurities present are only due to the uranium decay chain because as mentioned previously in this paper the AER of uranium decay chain is four times greater than the thorium decay chain. Moreover, we consider the secular equilibrium case. Secular equilibrium is a condition where all nuclei of the decay chain have the same activity. The aim of the simulation is to determine the quantity of $^{238}\mathrm{U}$ (in secular equilibrium) required to produce the corresponding AERs mentioned in Table II. For that, we simulate disintegrations in a layer (each material of Table II). The disintegrations result from 1 ppb of uranium and its daughter nuclei (secular equilibrium condition) distributed uniformly in different materials [7]. Few alpha particles are able to leave the layer and reach the detector. By considering a threshold energy for the detector, we have evaluated the corresponding contamination level of each materials reported in Table II.

IV. SER MONTE CARLO SIMULATION

In this section, the contribution of materials to SER is evaluated for a 65 technology by Monte Carlo method. The methods used to evaluate their involvement in SER are first explained for a 65 nm technology and then applied for the 45 and 32 nm node in Section V.

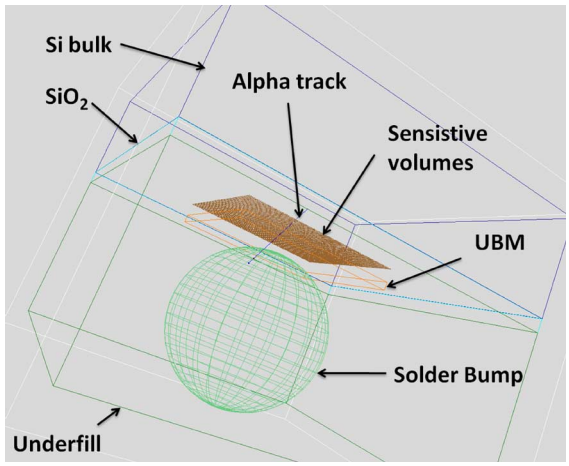

Fig. 3. Simulated geometrical structure generated by MC-ORACLE of a 65 nm technology node. As an indication of the scale, the sphere has diameter of 100 μm.

A. Simulated Structures for a 65 nm

By using Fig. 1, a geometrical structure in 3D is generated with MC-ORACLE for a 65 nm technology node in order to perform the simulations required. The simulated structure is presented in Fig. 3. The sphere represents the solder bump, the parallelepiped under the sphere and the shaded area under the parallelepiped represent, respectively, the UBM and the 140 $\times$ 140 simulated sensitive volumes. Since the cell area of a 65 nm is typically around 0.5 $\mu\mathrm{m}^2$, the distance between the sensitive volumes is about 0.71 μm (assuming a square cell).

The epoxy is represented by the volume containing the solder bump. The parallelepipeds under the UBM are the interconnect system and Si bulk, respectively. The bulk is represented by 60 μm of Si since that corresponds to the maximum range of the emitted alpha particles. The interconnect system is characterized by a 7 μm dielectric layer composed of SiO_2, the UBM layer is considered as a 5 μm Cu layer. Epoxy corresponds to the underfill, and the solder bump is represented by 100 μm of Pb-based solder.

B. Incertitude on the Number of Simulated SEU

In order to acquire precise results, enough alpha emission are simulated so that a few thousands of SEU are obtained (here, we took 3000 SEU). As Monte Carlo-based simulations are used, the incertitude on the number of SEU is the root square of the number of SEU. Consequently, as more than 3000 SEU are taken, the incertitude level is then lower than 2%.

C. Soft Error Rate Calculation for 65 nm Technology

According to Table II, the purity grades of silicon and copper are at the ULA level. Therefore, we assumed that the chip substrate (Si), the UBM (Cu) and the interconnects (SiO_2) are purity grade at ULA level (see Table II). As solder bumps have AERs in the UA to ULA range, three purity grades, the LA1 (upper limit of LA), LA2 (lower limit of LA) and ULA cases are considered. Moreover, the underfill layers are in the LA and

TABLE III
AER AND PURITY GRADE TAKEN FOR THE SIMULATION

Material	Purity grade	AER (α/cm^2-hr)$\times 10^{-4}$
Si	ULA	4
Cu	ULA	4
SiO_2	ULA	4
Solder bump	LA1, LA2, ULA	500, 20, 9
Underfill	LA3, ULA	40, 9

TABLE IV
CASES TAKEN FOR SIMULATIONS

CASE	Solder bump purity grade	Underfill purity grade
CASE 1	LA1	LA3
CASE 2	LA1	ULA
CASE 3	LA2	LA3
CASE 4	LA2	ULA
CASE 5	ULA	LA3
CASE 6	ULA	ULA

the ULA regions. Hence, two purity grades LA3 and ULA are considered. The AER taken for all materials taken in the simulations are presented in Table III.

Six cases reported in Table IV are studied. All cases have a constant emissivity for the Si (Bulk), Cu (UBM), SiO_2 (Interconnects).

Making the assumption of secular equilibrium, Monte Carlo simulations with MC-ORACLE are performed to calculate the SER associated with the contamination level of different materials in Table II. The RPP criterion is used to evaluate the SER of the 65 nm technology node. The sensitive volume and the critical charge of this technology are STMicroelectronics's parameters and are respectively 0.0035 μm^3 and 0.8 fC [20]. By assuming that sensitive volumes are cubes, the edge of a sensitive volume is thus 0.152 μm. As explained in Section II-B, we assumed that a presolder having a ULA purity grade is used so that diffusion of alpha emitting isotopes will not occur to the Si surface. In our simulations, isotopes of the uranium decay chain are uniformly distributed in each layer using their relative abundances compared to ^{238}U evaluated with MC-ORACLE (secular equilibrium assumption). All energies of alpha particles resulting from alpha emitting isotopes disintegrations of the uranium decay chain are considered [7].

Fig. 4 represents the contributions of the considered materials in the six studied cases. It is shown a constant SER due to Si bulk, Interconnects, and UBM. This is simply due to the fact that the ULA grade is always chosen for these materials. Therefore, the emissivity does not vary from a case to another for these materials. On the other hand, the materials used in the packaging are the most critical in triggering soft errors, depending on the purity of the solder bump and the underfill. According to our simulations, the use of a solder bump with an AER near the upper limit of LA (LA1) gives an unacceptable SER, leading to serious reliability issues. Moreover, in the LA classification, the range between the upper and the lower limit is so high that solder bump contribution to SER can change by a factor of 25.

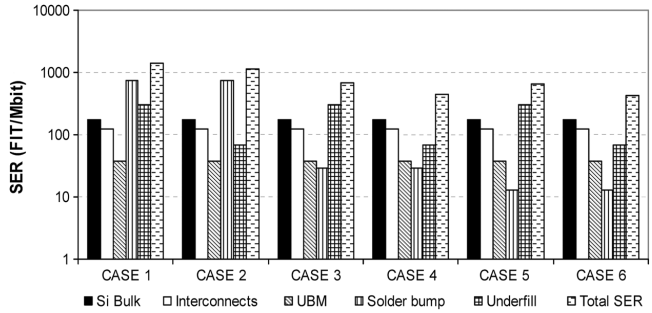

Fig. 4. Contribution to SER of different materials in a 65 nm flip chip device with different purity grades.

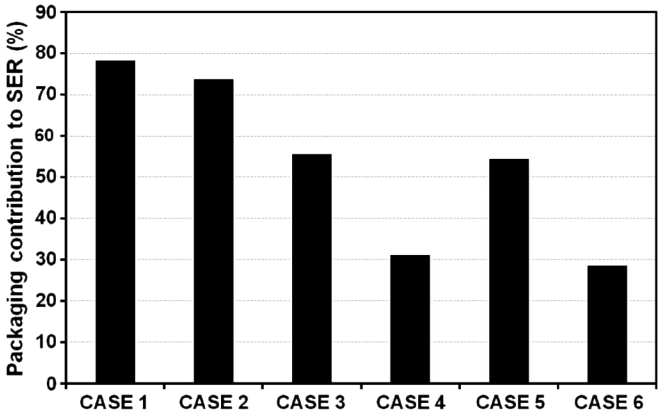

Fig. 5. Packaging contribution to alpha-SER in a 65 nm flip chip device in different cases.

However, when the solder bump has an AER near the lower limit of LA (LA2), the underfill becomes the main contributor to soft errors. The UBM, which is typically in the ULA range, contributes a negligible amount to the SER because of its small thickness (~ 5 μm). Therefore, among the package materials, the solder bump and the underfill are the most crucial, showing that care has to be taken (in the choice of purity grade of solder bumps and underfills) in order to reduce soft errors coming from the packaging system. Fig. 5 represents the percentage contribution of packaging materials to the SER. Its shows that at the ULA level, packaging materials have insignificant contributions to soft errors compared to other materials (see case 6 of Fig. 5). The overall contribution of packaging materials to SER is 28.5%. At this purity grade level, the bulk, even with an AER less than the packaging materials, contributes 42% of the soft errors induced by alpha particles. With this percentage, the silicon bulk becomes a great source of soft errors. The remaining 29.5% are due to the interconnect system. Work [6] reported the Alpha-SER from experiments of a 65 nm STMicroelectronics technology. In this same work the wafer and packages materials used have an AER of $(0.9 \pm 0.3) \times 10^{-3}$ α/cm^2.hr which is in the ULA grade for both wafer packages. Thus, this experiment is comparable to case 6. The experimental results of this work indicated that the Alpha-SER is 674 FIT/MBit. For case 6, the SER is 421 FIT/Mbit which is 37% lower than work [6]. The difference can be attributed to the fact that accurate emissivity of each material is not known, that we used a simplified

TABLE V
MCU CONTRIBUTION OF DIFFERENT MATERIALS

Material	Purity grade	MCU rate (FIT/Mbit)
Si bulk	ULA	7.66
Interconnects	ULA	7.56
UBM	ULA	0
Solder Bump	Any grade	0
Underfill	Any grade	0

TABLE VI
PARAMETERS USED FOR SIMULATIONS

Gate length (nm)	Sensitive volume (μm^3)	Sensitive volumes edge (μm)	Critical charge (fC)
45	0.0011	0.102	0.4
32	0.00037	0.072	0.2

model of a flip chip device and that we only considered the uranium decay chain whereas the thorium may play a role. From the ITRS roadmap, for a 6T-SRAM constituted with a 65 nm technology the SER requirement is 1150 FIT/Mbit including atmospheric neutrons contribution and other non radiation sources of soft errors [21]. According to our work, the alpha-SER represents approximately 37% of the requirement even at high purity grade of packaging materials and wafers. Furthermore, if an underfill of ULA level is not used (e.g. LA3: $4\times10^{-3}\,\alpha/\mathrm{cm}^2-\mathrm{hr}$), the minimum Alpha-SER increases to 660 FIT/Mbit which represents 57% of the SER specification required. As an indication, reference [6] gives, for the same technology with high purity materials, a neutron-SER of 359 FIT/MBit. The total SER for this technology is then 1019 FIT/Mbit which is comparable to the specification. This shows the importance of using ULA packaging materials.

D. MCU for a 65 nm Technology Node

MC-ORACLE was also used to simulate the MCU of the 65 nm technology node. Results are given in Table V for case 6 which corresponds to all material at ULA grade.

According to Table V, the Si bulk and the Interconnects have a MCU rate of 7.66 FIT/Mbit and 7.56 FIT/Mbit, respectively. The materials from the packaging do not significantly induce soft errors and no event has been seen in our simulations. The reason is that an alpha particle which is emitted from these materials has a very low probability to cross two sensitive volumes.

According to Table V, the variation of the purity grade of the packaging materials would not affect the MCU since these materials are very far from the sensitive volumes. However, the purity grade of the Si Bulk and the Interconnect is crucial for MCU for the reason that they are very close to sensitive volumes. By using Table V, we calculated the MCU ratio to SER rate in case 6 of Table IV. In this case, the MCU ratio to SER is 3%. Therefore, MCU due to alpha particles is negligible if a high pure Si bulk and Interconnect materials are used. Note that the underground experiment for the same technology found out a ratio of MCU to SER which is about 8% [6].

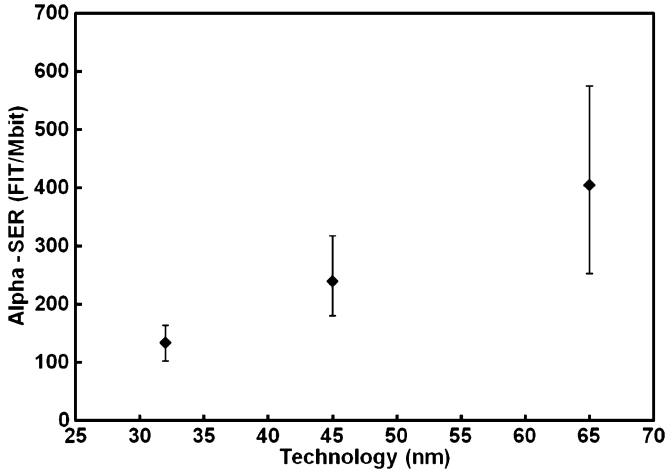

Fig. 6. SER induced by alpha particles for the 65, 45, and 32 nm technologies.

V. SER TREND FOR 45-nm AND 32-nm NODES

In this section, based on methods used in Section IV, the SER induced by alpha particles of a 45 and 32 nm are estimated. For that, we used parameters presented in Table IV. The cell distance used for a 45 and 32 nm technologies are, respectively, 0.50 μm and 0.35 μm. These distances are typical distances separating cells. Furthermore, the technologies studied in this section are composed of Si bulk and interconnects and we took an emissivity of $4\times10^{-4}\ \alpha/(\mathrm{cm}^2-\mathrm{hr})$. The emissivity of the packaging materials is $9\times10^{-4}\ \alpha/(\mathrm{cm}^2-\mathrm{hr})$. For the 45 and 32 nm technologies, the sensitive volumes and the critical charge are extrapolated based on work [20]. Results of this extrapolation are presented in Table IV.

Fig. 6 represents the SER and the contribution of the packaging to SER for the 65 nm, 45 nm, 32 nm technologies. According to Fig. 6, the SER due to alpha particles decreases with downscaling. The SER is reduced by a factor 3 from a 65 nm technology to a 32 nm technology node having the same AER. This can be explained by the shrinking and decrease of critical charge. Moreover, we represented the SER variation by bars in Fig. 6 in worst cases. The upward bars are due to a 20% increase of the sensitive volumes and a 20% decrease of the critical charge.

On the other hand, the downward bars are due to 20% decrease of the sensitive volumes and 20% increase of the critical charge. The SER length of the bars decreases as the technology decreases. This means for the future technologies, variations of critical charge and sensitive volume (20%) should only slightly change the SER. We have reached a point where the variation of the critical charge and sensitive volumes has a low impact on the SER. At this point, the probability of interaction of alpha particles and sensitive volumes decreases with scaling and variations of the critical charge would not change the SER level. It means that most of the alpha particles interacting with sensitive volumes induce soft errors since the critical charge is very low (0.2 fC is equivalent only to 1250 electron-hole pairs for a 32 nm). According to Fig. 7, the contribution of packaging materials to SER is constant as technology nodes decrease.

Therefore, the bulk and interconnect system are the dominant source of soft errors with a percentage of contribution which is

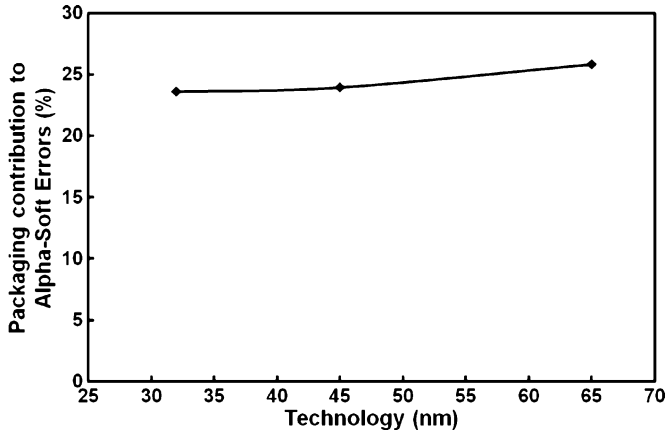

Fig. 7. Packaging contribution to SER for the 65, 45, and 32 nm technologies.

about 75% even with an emissivity two times lower than packaging materials. This is explained by their close location to sensitive volume and a high travel length of alpha particle in these materials.

VI. Conclusion

In summary, we have shown that materials within 60 μm from the die surface are the principal cause of soft errors if only high purity presolder layers are used. If that is the case, during processing radioactive impurities diffuse from the presolder layer near the surface of Si. In this paper, we determined that materials with 60 μm from the die in flip chip are the bulk, interconnect system, UBM, underfill, and the solder bump are responsible for emission of alpha particle capable of triggering soft errors. By assuming that an ULA presolder layer is used and secular equilibrium is reached, we evaluated the equivalent ^{238}U quantity in different materials used with a Monte Carlo method based on their alpha emission rate. Using the equivalent ^{238}U contamination level, simplified structures have been developed and the SER and MCU has been calculated for a 65 nm having a critical charge of 0.8 fC with a Monte Carlo tool called MC-ORACLE using the RPP criterion. Results showed that packaging is the crucial step that determines the SER level for the 65 nm technology and that solder bump and underfills are the most important material determining the SER. If these materials are not in the ULA, the alpha contribution to SER can drastically increase to an unacceptable level. We compared with the experimental SER measurement involving an ULA grade materials for a 65 nm technology. The comparison shows that our calculation has the same order magnitude than the result of the experiment. The difference is due to a simplified model and the non consideration of the thorium decay chain. Furthermore, we have illustrated the trends of SER for the 65, 45, and 32 nm technologies. The trends showed that the SER per Mbit decreases as technologies shrink. In addition, we explained that if package materials are at the ULA level, the materials used for FEOL and BEOL (bulk, metallization or interconnect) become the major sources of soft errors.

In the future, we shall consider not only the uranium but also the thorium decay chain which involves alpha particles with different energies and this should have an effect on the SER.

References

[1] J. F. Ziegler, "Terrestrial cosmic rays," *IBM J. Res. Develop.*, vol. 40, no. 1, pp. 19–40, Jan. 1996.
[2] R. Baumann, T. Hossain, S. Murata, and H. Kitagawa, "Boron compounds as a dominant source of alpha particles in semiconductor devices," in *IRPS Proceedings*, 1995, pp. 297–302.
[3] R. C. Baumann, "Soft errors in advanced semiconductor devices–Part I: The three radiation sources," *IEEE Trans. Device Mater. Rel.*, vol. 1, no. 1, pp. 17–22, Mar. 2001.
[4] R. C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 3, pp. 305–316, Sep. 2005.
[5] C. M. Timothy and H. W. Murray, "Alpha particles induced soft errors in dynamics memories," *IEEE Trans. Elec. Dev.*, vol. ED-26, no. 1, pp. 2–9, Jan. 1979.
[6] J. L. Autran, P. Roche, S. Sauze, G. Gasiot, D. Munteanu, P. Loaiza, M. Zampaolo, and J. Borel, "Altitude and underground real time SER characterization of CMOS 65 nm SRAM," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 4, pp. 2258–2266, Aug. 2009.
[7] F. Wrobel, F. Saigné, M. Gedion, J. Gasiot, and R D. Schrimpf, "Radioactive nuclei induced soft errors at ground level," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3437–3441, Dec. 2009.
[8] F. Wrobel, J. Gasiot, F. Saigné, and A. D. Touboul, "Effects of atmospheric neutrons and natural contamination on advanced microelectronic memories," *Appl. Phys. Lett.*, vol. 93, p. 064105, 2008.
[9] F. Wrobel, J. Gasiot, and F. Saigne, "Hafnium and uranium contributions to soft error rate at ground level," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3141–3145, Dec. 2008.
[10] M. Gedion, F. Wrobel, and F. Saigné, "Natural radioactivity consideration for high- κ dielectrics and metal gates choice in nanoelectronic devices," *J. Phys. D: Appl. Phys.*, vol. 43, no. 27, p. 275501, July 2010.
[11] R. Doering and Y. Nishi, *Handbook of Semiconductor Manufacturing Technology*. Boca Raton, FL: CRC Press, 2008, ch. 32.
[12] G. R. Blackwell, *The Electronic Packaging Handbook*. Boca Raton, FL: CRC Press, 2000, ch. 2.
[13] R. C. Jaeger, *Introduction to Microelectronic Fabrication*. Englewood Cliffs, NJ: Prentice-Hall, 2002, ch. 8.
[14] [Online]. Available: http://www.srim.org/
[15] R. Wong, S. J. Wen, P. Su, and L. Li, "Assessment of soft errors due to alpha emissions from presolder on flip chip devices," in *SEMINAR on Impact of Packaging Materials and Processes on Device Soft Error Rates*, San Jose, CA, Oct. 2009.
[16] A. Tseng, "ULA dedicated line for FC BGA," in *SEMINAR on Impact of Packaging Materials and Processes on Device Soft Error Rates*, San Jose, Oct. 2009.
[17] *Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices*, JESD89A, JEDEC Standard, Oct. 2006, pp. 78.
[18] B. Clarck, "Progress towards standardization of alpha flux measurements in electronic materials," in *SEMINAR on Impact of Packaging Materials and Processes on Device Soft Error Rates*, Oct. 2009.
[19] F. Wrobel and F. Saigne, "MC-ORACLE: A tool for predicting soft error rate," *Comput. Phys. Commun.*, 2010, doi:10.1016/j.cpc.2010.10.005.
[20] P. Roche, G. Gasiot, K. Forbes, V. O'Sullivan, and V. Ferlet, "Comparisons of soft error rate for SRAMs in commercial SOI and bulk below the 130 nm technology node," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 2046–2054, Dec. 2003.
[21] [Online]. Available: http://www.itrs.net/