Microelectronics Reliability 50 (2010) 1822–1831

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Soft-errors induced by terrestrial neutrons and natural alpha-particle emitters in advanced memory circuits at ground level

J.L. Autran [a,*], D. Munteanu [a], P. Roche [b], G. Gasiot [b], S. Martinie [a], S. Uznanski [a,b], S. Sauze [a], S. Semikh [c], E. Yakushev [c], S. Rozov [c], P. Loaiza [d], G. Warot [d], M. Zampaolo [d]

[a] IM2NP – CNRS, Aix-Marseille University, 49 rue Joliot Curie, F-13384 Marseille Cedex 13, France
[b] STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles Cedex, France
[c] Dzhelepov Laboratory of Nuclear Problems, JINR, 141980 Dubna, Moscow region, Russia
[d] LSM, CEA-CNRS, Carré Sciences, 1125 route de Bardonnèche, F-73500 Modane, France

ARTICLE INFO

Article history:
Received 1 July 2010
Accepted 13 July 2010
Available online 11 August 2010

ABSTRACT

This review covers our recent (2005–2010) experiments and modeling-simulation work dedicated to the evaluation of natural radiation-induced soft errors in advanced static memory (SRAM) technologies. The impact on the chip soft-error rate (SER) of both terrestrial neutrons induced by cosmic rays and alpha-particle emitters, generated from traces of radioactive contaminants in CMOS process or packaging materials, has been experimentally investigated by life (i.e. real-time) testing performed at ground level on the Altitude Single-event Effect Test European Platform (ASTEP) and underground at the underground laboratory of modane (LSM). The paper describes these two test platforms and surveys the characterization results obtained for two SRAM technology nodes (130 nm and 65 nm). Experimental results concerning the characterization of the natural radiation environment are also reported.

1. Introduction

Soft-errors induced by natural radiation are considered as one of the most important primary limits for modern digital electronics reliability [1,2]. The problem has been well-known for space applications over many years (more than 40 years) and production mechanisms of single-event effects (SEE) in semi-conductor devices by protons or heavy ions well apprehended, characterized and modeled [2–4]. In a similar way for avionic applications, the interactions of atmospheric neutrons with electronics has been identified as the major source of SEE, distinguishing thermal neutrons (interacting with ^{10}B isotopes potentially present in circuit materials, but progressively removed from technological processes [5]) and high-energy atmospheric neutrons (up to the GeV scale) [3]. For the most recent deca–nanometers technologies, the impact of other atmospheric particles produced in nuclear cascade showers on circuits has been clearly demonstrated (protons [6]) or is still an open question for some exotic particles (pions and charged muons [7–9]). With respect to such high-altitude atmospheric environments, the situation at ground level is slightly different. Of course, atmospheric neutrons are always the primary particles but, with a flux approximately divided by a factor ~300 at sea-level with respect to the flux at avionics altitudes, the soft-error rate (SER) of circuits can be now affected by a third additional source of radiation, usually neglected because completely screened by neutrons in avionics: the alpha particles generated from traces of radioactive contaminants in CMOS process or packaging materials [10,11]. As a consequence of these multiple sources of radiation, the accurate characterization of the SER of circuits at ground level is rather a complex task because one can clearly separate the contribution to SER of atmospheric particles (the external constraint) from the one due to natural alpha-particle emitters present as contaminants in circuit materials (the internal constraint) [1].

In this context, the present work surveys our 2005–2010 experiments and modeling-simulation works [12–17] dedicated to the evaluation of natural radiation-induced soft errors in advanced static memory (SRAM) technologies following a real-time (i.e. life testing) approach. The paper is organized as follows. In Section 2, we present in details the two test platforms developed and installed, both in altitude and underground, to perform real-time characterization of circuits. Experimental results concerning the characterization of the natural radiation environment are also reported. Section 3 gives some details concerning then different setups (hardware and software) developed to remotely perform real-time testing of SRAM circuits manufactured in 130 nm and 65 nm technologies. Section 4 summarizes the main real-time characterization results obtained these last years for these different experiments and analyzes data in terms of soft-error rate and of separation of neutron and alpha-particle emitter contributions

* Corresponding author. Address: IM2NP – UMR CNRS 6242, Bâtiment IRPHE – BP 146, 49 rue Joliot Curie, F-13394 Marseille Cedex 13, France. Tel.: +33 (0) 4 96 13 97 17; fax: +33 (0) 4 96 13 97 09.
E-mail address: jean-luc.autran@univ-provence.fr (J.L. Autran).

0026-2714/$ - see front matter © 2010 Elsevier Ltd. All rights reserved.
doi:10.1016/j.microrel.2010.07.033

to the circuit SER. Finally Section 5 presents the modeling and simulation recently developed to reproduce real-time experiments and to extract alpha-particle emitter contamination levels from data obtained in cave experiments. In conclusion, we indicate some near and middle terms perspectives for this work.

2. The altitude and underground test platforms

In order to perform real-time characterizations of circuit in natural environments, we developed and installed two complementary test platforms, the first one in altitude on the Plateau de Bure (French south Alps) in 2005 (to evaluate the impact of atmospheric neutrons on electronics), the second one inside the underground laboratory of modane in 2007 (to measure the SER induced by radioactive contaminants). In the following, we briefly describe this two test platforms, their radiation environments and the main instruments used to characterize the background radiation.

2.1. The altitude SEE test European platform (ASTEP)

ASTEP is a permanent installation and a dual academic research/R&D platform founded by STMicroelectronics, JB R&D and L2MP-CNRS in 2004 [12]. The platform is referenced as a research location in the international JEDEC standard JESD89A [18] and is currently operated by IM2NP-CNRS (formerly L2MP). ASTEP is located in the French Alps on the desert Plateau de Bure (Devoluy Mountains) at 2552 m (Latitude North 44°38′02″, Longitude East 5°54′26″), in a low electromagnetic noise environment, and is hosted by the Institute for Radio-astronomy at Millimeter Wavelengths (IRAM). It has been fully operational since March 2006. From a geomagnetic point-of-view, the ASTEP site is characterized by a cutoff rigidity of 5 GV; the natural neutron flux is approximately six times higher that the reference flux measured at New-York City. This value (also called "acceleration factor" with respect to the gain that we can expect on the duration of real-time experiments performed in altitude instead of at sea-level) has been precisely measured in 2008, as explained in the following. Fig. 1a and b shows a general view of the Plateau de Bure (IRAM observatory) and an external view of the ASTEP building respectively; the building extension (first-floor) was finished in 2008 and has been hosted, since July 2008, the Plateau de Bure Neutron Monitor (PdBNM). This instrument was designed and constructed in 2007 to survey in real-time (1 min integration time) the time variations of the natural neutron flux incident on the ASTEP platform and on the dedicated SER experiments. The PdBNM, shown in Fig. 2, is a super 3-NM64 neutron monitor based on three high pressure (2280 Torr) cylindrical He^3 detectors (model LND 253109). Each tube is surrounded by a 25 mm coaxial polyethylene tube (neutron moderator) and by coaxial thick (50 mm) lead rings (secondary neutron producers); all these elements are placed inside a 80 mm thick polyethylene box to reject low energy (thermal) neutrons produced in the close vicinity of the instrument. A Canberra electronic detection chain composed of three charge amplifiers model ACHNP97 and a high voltage source 3200D) was chosen in complement to a Keithley KUSB3116 acquisition module for interfacing the neutron monitor with the control PC. The design and the construction of the PdBNM followed the recommendations published in [19,20] for the optimization of the apparatus response. Fig. 3 shows the PdBNM averaged response (one point per hour) from August 1, 2008 to June 21, 2010. This uncorrected response from atmospheric pressure directly gives an image of the neutron flux variation at the ASTEP location, evidencing ~30% variations of this averaged flux at ground level essentially due to atmospheric pressure variations. During its installation, the PdBNM was used to experimentally determine the acceleration factor (AF) of the ASTEP location with respect to sea-level. Assembled and previously operated in Marseille during the year 2007–2008, the PdBNM was transported and installed on the Plateau de Bure in July 2008. With strictly the same setup, two series of data were thus recorded in Marseille and on the Plateau de Bure: the difference between the counting rates and barometric coefficients for the two locations allowed us to directly evaluate the acceleration factor of ASTEP with respect to Marseille location, here estimated to 6.7 [21]. Taking into account latitude, longitude and altitude corrections for Marseille location with respect to New-York City (the reference place in the world for standardization purposes), the final value of the acceleration factor is $AF = 6.7 \times 0.94 \approx 6.3$. This value is close to 6.2, the average acceleration factor reported in the Annex A of the JEDEC standard JESD89A [18,22] and close to 5.9, the value given by the Qinetic Radiation Atmospheric

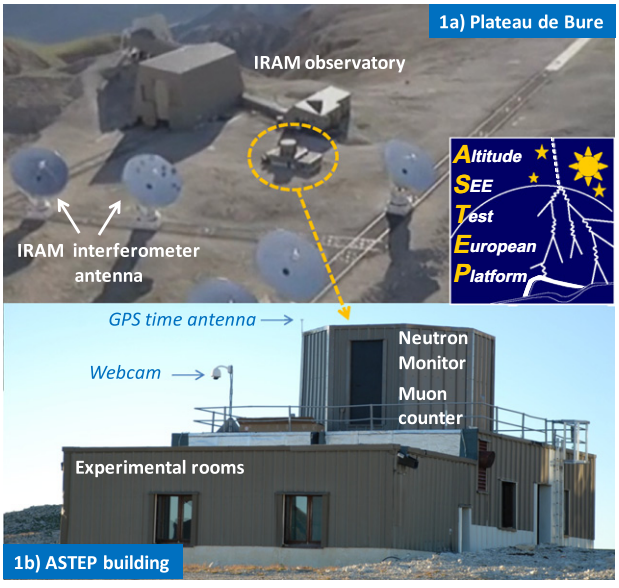

Fig. 1. (a) General view of the Plateau de Bure. (b) External view of the ASTEP building showing the new extension (first-floor) designed to host the Plateau de Bure neutron monitor (PdBNM).

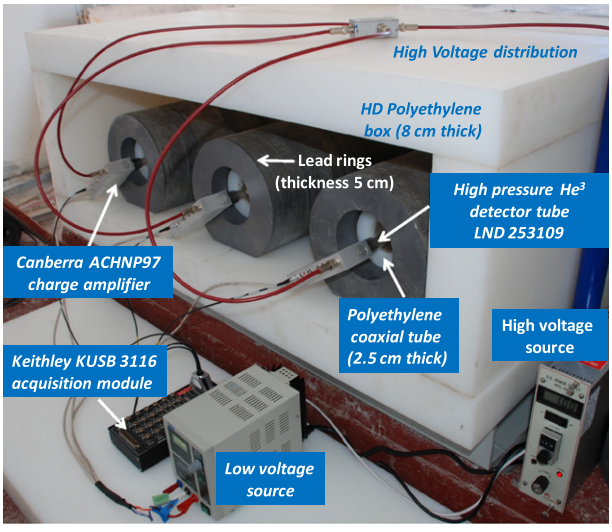

Fig. 2. Detailed view of the PdBNM showing the extremities of the cylindrical neutron detector tubes connected to the charge amplifiers and to the acquisition module (electronic counters).

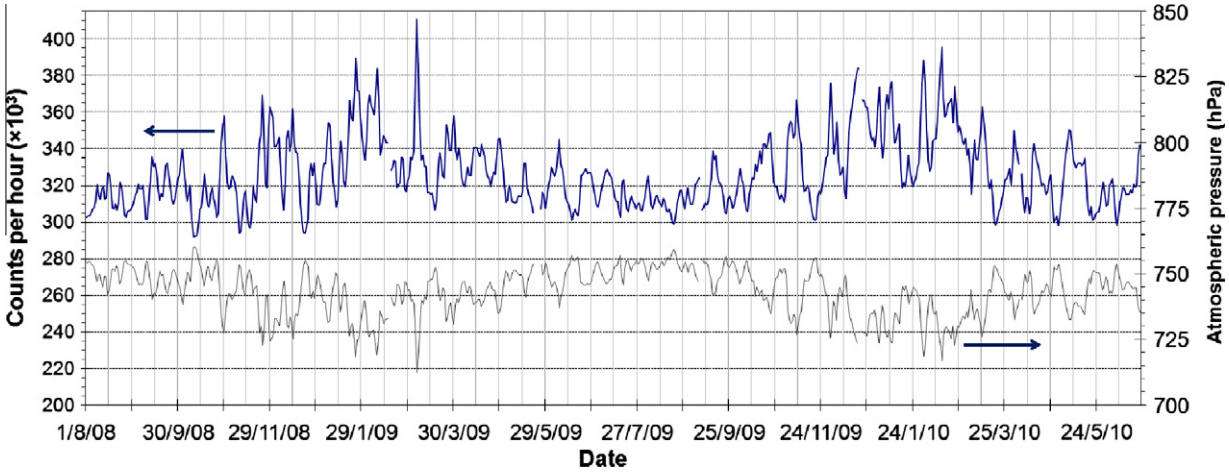

Fig. 3. Plateau de Bure neutron monitor response recorded from August 1, 2008 to June 21, 2010. Data are uncorrected from atmospheric pressure and averaged over 1 h. ~30% variations in neutron flux are evidenced, with two peaks (around 4×10^5 counts/h) corresponding to the passage of two severe atmospheric depressions (the first peak correspond to the Klaus storm on January 25, 2009).

Model (QARM) [23,24] for quiet sun activity. The experimental value AF = 6.3 will thus be considered as the acceleration factor value characterizing the ASTEP location.

2.2. The underground laboratory of modane (LSM)

In October 2007, we deployed a new test platform in the underground laboratory of modane (LSM) in order to obtain complementary measurements for separating the contribution to SER of atmospheric particles from the one due to natural alpha-particle emitters. This laboratory is located about 1700 m under the top of the Fréjus mountain (4800 m water equivalent), near the middle of the Fréjus highway tunnel connecting France and Italy [25]. It was created in 1983 in order to conduct particle physics and astrophysics experiments in a strongly reduced cosmic ray background environment. Due to the depth of the LSM, the average particle flux inside the laboratory is extremely reduced [26]: about 4 muons/m^2/day corresponding to a two million reduction factor compared to the flux at sea-level; a few 10^3 fast neutrons/m^2/day (depending on the neutron energy and the measurement location in the laboratory) emitted by natural radioactivity from the rock, the neutron component of cosmic rays being totally eliminated at this depth. In addition, the Radon in the laboratory is maintained at a very low rate of ~20 Bq/m^3 owing to an air purification system which totally renews the volume of the air inside the laboratory twice an hour. Recent fast and thermal neutrons measurements have been performed by Yakushev [27] at immediate proximity of our setups (see Fig. 4); these results have then been modeled and reproduced within a few percents by calibrated Geant4 Monte-Carlo simulations. They give a flux of fast neutrons with $E > 0.3$ eV (cadmium threshold) of $\sim 3 \times 10^{-6}$ neutron/cm^2/s. Measurements of thermal neutrons at the same place with bare He^3 filled proportional counter gave $\sim 2 \times 10^{-6}$ neutron/cm^2/s. Knowing that flux of fast and thermal neutrons are connected, Monte-Carlo predicted coefficient for really fast neutrons with $E > 0.5$ MeV to thermal neutrons ($E < 0.3$ eV) is about 0.64–0.66 (depends slightly on rock and concrete). Thus we can estimate the number of such neutrons ($E > 0.5$ MeV) at place of SER experiments from this as $\sim 1.2 \times 10^{-6}$ neutron/cm^2/s. These measurements confirm the residual background value of only a few 10^3 fast neutrons/m^2/day inside the experimental room deduced from experimental measurements and resulting from simulation work [28]. With an excellent confidence, we consider for future data analysis that all events detected at LSM during the SER real-time experiments are induced by internal chip radioactivity (alpha-particle emitters) and not by the external neutron background.

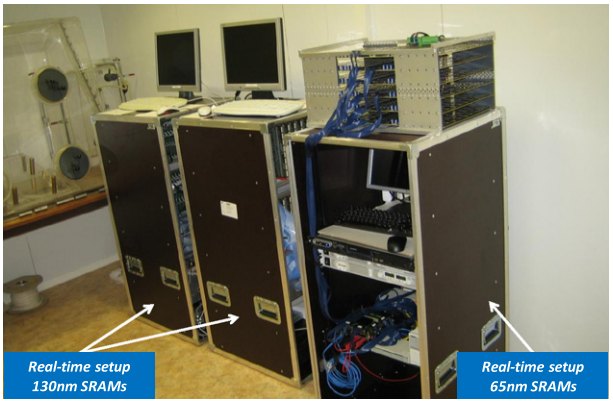

Fig. 4. General view of the experimental room dedicated to microelectronics experiments inside the Modane underground laboratory. The two automatic test equipments are dedicated to the real-time SER test of 130 nm and 65 nm SRAM circuits.

3. Real-time experimental details

3.1. SRAM circuits under test

Real-time measurements have been performed on bulk SRAMs fabricated by STMicroelectronics using commercial CMOS processes in 130 nm (200 mm wafers) and 65 nm (300 mm wafers) technologies. These processes are based on a Boro-Phospho-Silicate Glass (BPSG)-free Back-End Of Line (BEOL) which eliminates the major source of ^{10}B in the circuits and drastically reduces the possible interaction between ^{10}B and low energy neutrons (in the thermal range and below) [5,29,30]. The test vehicle for the 130 nm technology is composed of 4 Mbit Single Port SRAM (SP-SRAM) with a bit cell area of 2.50 μm^2. A total of 3664 Mbit was considered for real-time experiments, both in altitude (ASTEP) and underground (LSM). For the 65 nm technology, the test chip contains 8.5 Mbit of SP-SRAM (bit cell area of 0.525 μm^2) and 1 Mbit of Dual Port SRAM (DP-SRAM, bit cell area of 0.98 μm^2). The SP-SRAM bitcell for the 65 nm technology node, corresponds to the standard six transistors SRAM designed with one access

transistor on each internal node. DP-SRAM has the same electrical schematic with two additional access transistors, one on each side of the memory, giving the ability to simultaneously read and write different memory cells at different addresses. No deep N-well [11] was used in both 130 and 65 nm devices tested in the present work. Both 130 nm and 65 nm bitcells were fully modeled with 3D TCAD tools (Sentaurus Synopsys package [31]) to evaluate their sensitivity to heavy ions and to determine the SEU/SBU and MBU/MCU occurrences as a function of ion parameter [32–34]. In complement to TCAD work, numerous experimental studies were conducted these four last years to characterize the different test chips from an accelerated-test point-of-view with neutrons at the Los Alamos Neutron Science Center (LANSCE), as well as with an intense Am^{241} alpha source at STMicroelectronics [14,15].

3.2. Hardware and software setups

Two different SER test equipments, specially designed for the study, have been developed and assembled by Bertin Technologies (Aix-en-Provence, France) for the 130 nm devices [14–16] and by iRoC Technologies (Grenoble, France) for the 65 nm ones [17], respectively. Fig. 4 shows a general view of these test equipments currently deployed at LSM. The 130 nm setup was successively installed on ASTEP during the period [March 31, 2006–November 6, 2006], then transported to the LSM and installed on October 16, 2007. For the 65 nm experiment, two identical setups were constructed; they were installed on ASTEP on January 21, 2008 and at LSM on April 11, 2008. The three setups are working since these respective dates at room temperature, except for the altitude 65 nm setup which was stopped on May 5, 2009 and restarted on June 26, 2010 for high temperature measurements performed at 85 °C (the stack of motherboards was placed into a computer-controlled heating oven).

In the present configuration, each system is capable of monitoring several hundred of chips (1280 chips for the 130 nm setup and 384 chips for the 65 nm one) and performing all requested operations such as writing/reading data to the chips, comparing the output data to the written data and recording details on the different detected errors in SRAM chips. The different hardware and software components have been designed to strictly follow all the specifications of the JEDEC Standard JESD89A [18]. In particular, the design of the setup ensures that all detected errors come from the devices under test, not from external or system noise, by respecting strict design and construction guidelines explained in Refs. [18,35]. A special test algorithm used for SRAM testing [15] has been developed in complement to hardware aspects to detect and discriminate SBU from MCU, Single-Event Functional Interrupt (SEFI) or Single-Event Latchup (SEL) events. Current consumption of all power lines provided by the tester is monitored and logged during the test. User can see in real-time the errors on the monitor of the tester; automatic alert message emission by the tester or totally remote control operation can be also envisaged for a continuous test survey in other location outside LSM.

4. Experimental results and data analysis

We present in this section our most recent and updated results obtained for the 65 nm technology (Single Port SRAM circuits) from real-time in altitude and underground. Comparison with real-time data obtained for the 130 nm technology (SP-SRAM) is also reported. In the following, all numerical results have been normalized by a common arbitrary scaling factor, set lower than 3×. The real order of magnitude for the reported data is thus not significantly altered.

4.1. Altitude and underground real-time experiments

Fig. 5 shows the cumulative number of fails detected in SP-SRAMs versus test duration (expressed in Mbit × h) for both altitude measurements (successively performed at room temperature and at 85 °C) and underground one (performed at room temperature). Because the measurements started (and stopped for the altitude test) at different dates, the number of Mbit × h cumulated in the different experiments are not identical.

A data analysis summarized in Table 1 shows that for the altitude experiment a total of 61 events involving a total of 97 cell upsets or bit flips was detected for SP-SRAM at room temperature (respectively 52 events and 66 bit flips for the test at high temperature) including 44 SBU and 17 MCU (respectively 44 SBU and 7 MCU). These MCUs involves a total of 53 bit flips (respectively 22 at 85 °C) which are physical adjacent bit cells in all cases with a multiplicity ranging from 2 to 7. The distribution of these MCUs is given in Fig. 6 for the three series of measurements. Note the importance of MCU mechanisms in such a deep submicron technology: for example in altitude at room temperature, this MCU contribution represents $17/61 \cong 28\%$ of the detected events but, in the same time, 53/97 = 54.6% of the total number of detected bit flips. For the cave experiment and due now to a very satisfactory statistics (with respect to the first results published in 2009, see Ref. [15]), 51 events were recorded, corresponding to 38 SBU and 13 MCU with multiplicities of 2–5. The fraction of MCU is found equal in this case to $13/51 \cong 25.5\%$ of the detected events and to 36/74 = 48.6% of the total number of detected bit flips. Altitude and underground experiments visibly lead to very similar fractions of SBU and MCU with respect to the total of events and bit flips; this result contrasts with the first tendencies previously reported for this 65 nm technology [15]. Another remark concerns the impact of the temperature for altitude tests: we observe in both cases in Fig. 5, i.e. for room temperature and high (85 °C) temperature tests, very similar bit flip occurrence distributions with an identical and constant slope, demonstrating here (and at this level of statistics for the high temperature test) the non-dependence of the soft-error rate with temperature for the present 65 nm technology. It is also clear that such heating level has no impact on the occurrence of latchup or micro-latchup; any such events is detected for all experimental condition in altitude and underground, demonstrating the latchup immune character of this technology with single-port SRAM cell architecture.

From data of Fig. 5 for the three experiments, we estimated the real-time SER at the test location, reported in Table 1, using the well-known formula:

$$\mathrm{SER} = \frac{N_r}{\Sigma_r} \times 10^9 \ (\mathrm{FIT/Mbit}) \tag{1}$$

where N_r is the number of bit flips (for flip SER), SBU (for SBU SER) or MCU events (for MCU SER) observed at time T_r and Σ_r is the number of Mbit × h cumulated at time T_r.

We also reported in Table 1 the upper and lower confidence intervals at 90% level based on the χ^2 distribution in order to estimate the experimental error margins [18]. Due to the long duration of the experiments and specially for the underground experiment (5.98×10^7 cumulated Mbit × h), the averaged slope of the bit flip distribution, shown in Fig. 5 (dotted line), can be correctly estimated, even if large multiplicity events are present. It was not completely the case for previous estimations reported in 2009 [15]. The consequence is that the total flip SER for the underground experiment has to be reevaluated to ~1040 FIT/Mbit with respect to the previous first estimation around 740 FIT/Mbit. From this example, we point out here one important limitation of real-time experiments for deep submicron or deca–nanometer technologies: with the growing importance of MCU events, test durations must

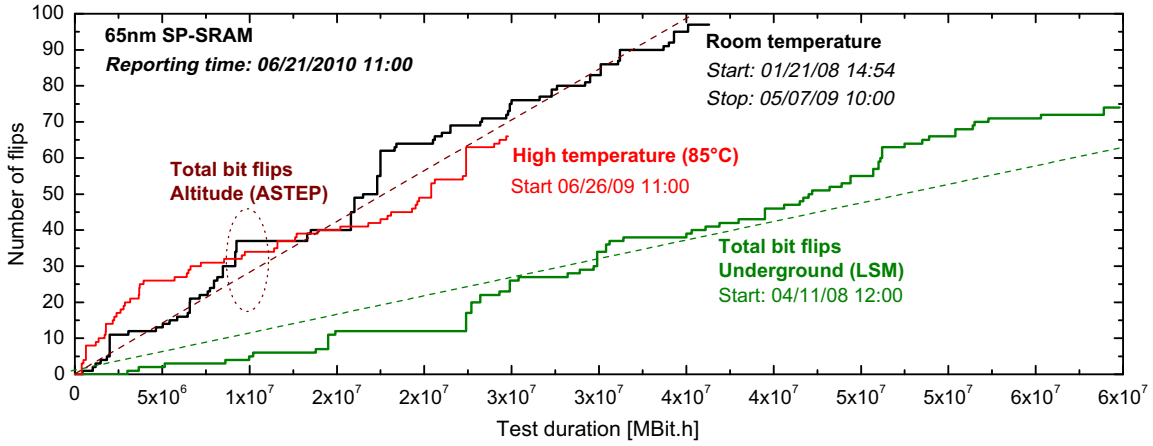

Fig. 5. Cumulative total fails (i.e. total bit flips) versus test duration for the 65 nm SP-SRAM during both altitude and underground experiments. Test has been conducted under nominal conditions: V_{DD} = 1.2 V, standard checkerboard test pattern and room temperature (except for the high temperature test conducted at 85 °C using a heating oven).

Table 1
Summary and key-values for the real-time 65 nm experiments conducted in altitude and underground.

Altitude experiment – 65 nm	Room (21 °C) temperature	High (85 °C) temperature
Starting date	01/21/08 14:54	06/26/09 13:04
Reporting date	05/07/09 10:00	06/21/10 8:00
Cumulated number of Mbit × h	3.63×10^7	2.48×10^6
Total number of events/bit flips	61/97	52/66
Number of SBU	44	44
Number of MCU/MCU flips	17/53	7/22
Number of latchup/micro-latchup	0	0
SBU SER on ASTEP (FIT/Mbit)	1212	1774
MCU SER on ASTEP (FIT/Mbit)	468	282
Total flip SER on ASTEP (FIT/Mbit) (*from averaged distribution slope*)	2670	2670
Lower (10%) and upper (90%) confidence limits (FIT/Mbit)	3313, 2211	3313, 2211
Underground experiment – 65 nm		
Starting date		04/11/08 12:00
Reporting date		21/06/10 11:00
Cumulated number of Mbit × h		5.98×10^7
Total number of events/bit flips		51/74
Number of SBU		38
Number of MCU/MCU flips		13/36
Number of latchup/micro-latchup		0
SBU SER (FIT/Mbit)		635
MCU SER (FIT/Mbit)		217
Total flip SER (FIT/Mbit) (*from averaged distribution slope*)		1040
Lower (10%) and upper (90%) confidence limits (FIT/Mbit)		1280, 845

be significantly increased to average MCU (rare) events of large multiplicities and to reflect the correct soft-error rate. Concerning the altitude test, the total flip SER is evaluated in the same way to 2670 FIT/Mbit, which is close to the previous reported value (2934 FIT/Mbit). This 10% decrease is also due to this MCU impact on the SER extraction. Finally, the calculation of the normalized neutron real-time SER at the reference location of New-York City (NYC) is obtained from the following expression, assuming that the fail rate due to alpha-particles is identical to the alpha-SER experimentally deduced from underground experiment:

$$\begin{cases} \text{neutron-SER}|_{NYC} = \frac{\text{SER}|_{ASTEP} - \text{SER}|_{LSM}}{AF} \\ \text{alpha-SER}|_{NYC} = \text{SER}|_{LSM} \end{cases} \quad (2)$$

In Eq. (2), the value of the acceleration factor of the ASTEP site is taken equal to AF = 6.3, the experimental value determined from data collected using the Plateau de Bure neutron monitor. The normalized neutron-SER is then equal to (2670–1040)/6.3 ≈ 260 FIT/Mbit and the total flip SER for both alpha and neutron contributions is equal to 1040 + 260 = 1300 FIT/Mbit for the 65 nm SP-SRAM.

4.2. Accelerated tests

In complement to real-time measurements, accelerated tests using an intense alpha-particle Am^{241} source and a neutron-beam have been performed on several 65 nm chips taken randomly from the same fabrication lot than circuits tested in altitude and underground (see Refs.[14,15] for experimental details). For alpha-particle test, the reported SER values have been extrapolated to a nominal alpha flux of 0.001 alpha/cm^2/h. This value emulates the alpha emissivity rate for the semi-conductor processing and packaging materials with an "ultra-low alpha" grade. Experimental measurements led to an accelerated alpha-SER = 605 FIT/Mbit for SP-SRAM. In a similar way, accelerated neutron-SER measurements conducted at the LANSCE WNR facility have been extrapolated to the reference (NYC) neutron integrated flux of 13 neutrons/cm^2/h: we obtained a value of 470 FIT/Mbit for SP-SRAM.

The combination of real-time and accelerated alpha-SER values will allow us to estimate the alpha-particle emission rate for the semi-conductor processing and packaging materials, as explained in Section 4.3. Concerning neutron-SER, the comparison between real-time (240 FIT/Mbit) and accelerated (470 FIT/Mbit) values (normalized at the reference location New-York City) shows a discrepancy within a factor 2 between the two approaches; this remains very acceptable with respect to dosimetry errors and/or statistical dispersions from sample-to-sample, lot-to-lot and error intervals on the knowledge of some physical, technological and electrical key-parameters (manufacturing variability) [1,36]. Moreover, this result could be explained by possible differences between the neutron-beam and the real atmospheric neutron spectra, largely introduced by the cutoff energy of the accelerator which is always well below cosmic ray energies. This could be also confirmed by the relatively important difference in the percentages of bit flips involved in MCU events for the two experiments: 53.5% for real-time and 31% for accelerated tests. Our recent results concerning heavy ion testing and 3D simulations of MCU occurrence in 65 nm SRAMs [13] are coherent with this observation:

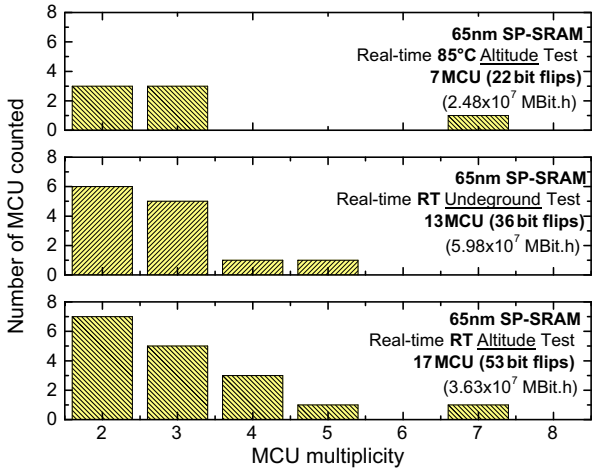

Fig. 6. Distribution of the MCU multiplicity (i.e. number of bit flips per MCU event) for the 11 MCU events detected during the altitude test (SP-SRAM). These MCUs involves a total of 38 bit flips which correspond to physical adjacent bit cells (in the memory plan) in all cases.

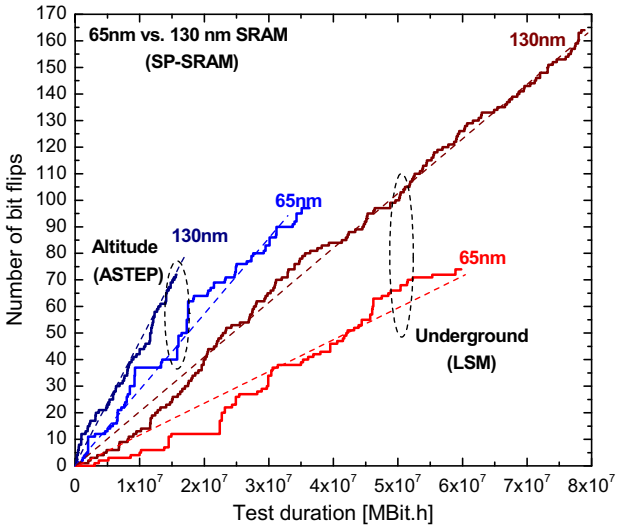

Fig. 7. Cumulative total fails versus test duration for both 130 nm and 65 nm SP-SRAMs detected in altitude and underground. Test has been conducted under nominal conditions for both technologies: V_{DD} = 1.2 V, room temperature, standard checkerboard test pattern. For 130 nm data, experiment periods are [March 31, 2006–November 6, 2006] for the altitude test and [October 16, 2007–November 24, 2008] for the underground test.

the contribution of MCU to the total number of upsets strongly increases with the LET of the incident ion, suggesting that high energy neutrons (indirectly inducing a non-negligible fraction of high LET ions) play a major role in the occurrence of large size MCUs effectively observed in real-time experiments.

4.3. Comparison with 130 nm SRAM technology

Fig. 7 shows a direct comparison of the total bit flip distributions versus test duration for the two SRAM technologies. For the 130 nm, we report here an exceptional long duration (more than 2 years) underground test which allows us to accurately extract the alpha-SER of this technology. Data analysis concerning both altitude and cave experiments are summarized in Table 2. A total of 72 bit flips was detected after 1.55×10^7 Mbit × h in altitude, 164 fails after 7.89×10^7 Mbit × h during the underground test. The analysis of Fig. 7 indicates that, for both test locations, the 130 nm technology exhibits a higher soft-error rate (directly linked to the slope of the curves) than the 65 nm one. In addition, for the altitude test, 5 MCU events, involving each 2 physical adjacent bit cells, were recorded; no MCU event was detected for the cave experiment. This difference in MCU occurrence for the two technologies is clearly highlighted by the "staircase shape" of the curves: the 130 nm distribution has very regular stairs (each stair corresponding to a single bit flip), at the opposite, the 65 nm curves exhibits irregular and marked stairs, which corresponds to a kind of "visual signature" of MCU events. These SER values related to the 130 nm technology are reported in Fig. 8. We used Eq. (2) to separate alpha from neutron contributions to the total normalized SER value. Fig. 8 also summarizes the key-values of experimental real-time SER for both 130 and 65 nm technologies (SP-SRAM). Alpha-SER is found to decrease by a factor ~2 for the 65 nm technology with respect to the 130 nm one and neutron-SER by a factor 1.6, resulting in a net improvement of the total SER by a factor ~1.9.

Table 2
Summary and key-values for the real-time 130 nm experiments conducted in altitude and underground.

130 nm SRAM technology	Altitude (ASTEP) test	Underground (LSM) test
Starting date	03/31/06	10/16/07 14:22
Reporting date	11/06/06	06/21/10 8:00
Cumulated number of Mbit × h	1.55×10^7	7.89×10^7
Total number of events/bit flips	67/72	164/164
Number of SBU	62	164
Number of MCU/MCU flips	5/10	0/0
Number of latchup/micro-latchup	0	0
SBU SER on ASTEP (FIT/Mbit)	4000	2079
MCU SER on ASTEP (FIT/Mbit)	323	0
Total flip SER on ASTEP (FIT/Mbit)	4658	2079
Lower (10%) and upper (90%) confidence limits (FIT/Mbit)	5590, 3788	2367, 1831

4.4. Estimation of the alpha-particle emission rate

Combining real-time and accelerated alpha-SER values, for a given technology, allows us to estimate the alpha-particle emission rate for the semi-conductor processing and packaging materials. Because accelerated values are extrapolated (i.e. normalized) to the reference value of 0.001 alpha/cm^2/h (that corresponds to an "ultra-low alpha" grade [5]), the real alpha-particle emission rate is simply given by this value multiplied by a factor corresponding to the ratio of the real-time SER by the accelerated SER. We thus obtain for the 65 nm technology $0.001 \times (1040/605) \approx 1.7 \times 10^{-3}$ alpha/cm^2/h. For the 130 nm technology, a similar calculation from real-time SER value given in Fig. 7 and considering the accelerated value of 380 FIT/Mbit reported in Ref. [14] gives: $0.001 \times (380/1530) \approx 4.0 \times 10^{-3}$ alpha/cm^2/h. In addition to this indirect extraction of the alpha-particle emissivity via SER tests, the alpha emission rates for both the tested wafers and packages (mold compound) were accurately characterized using an ultra-low alpha background counter (gas flow type). The tests were performed in a dedicated characterization lab at STMicroelectronics. A high purity in terms of radioactive contaminants was confirmed, around $(0.9 \pm 0.3) \times 10^{-3}$ alpha/cm^2/h for the 65 nm technology. In parallel, the same measurement procedure was applied for the characterization of wafers and packages of the 130 nm technology. An emissivity level of $(1.1 \pm 0.2) \times 10^{-3}$ alpha/cm^2/h was measured on a first wafer, the value of $(2.3 \pm 0.2) \times 10^{-3}$ alpha/cm^2/h was measured on a second wafer from another lot, confirming with

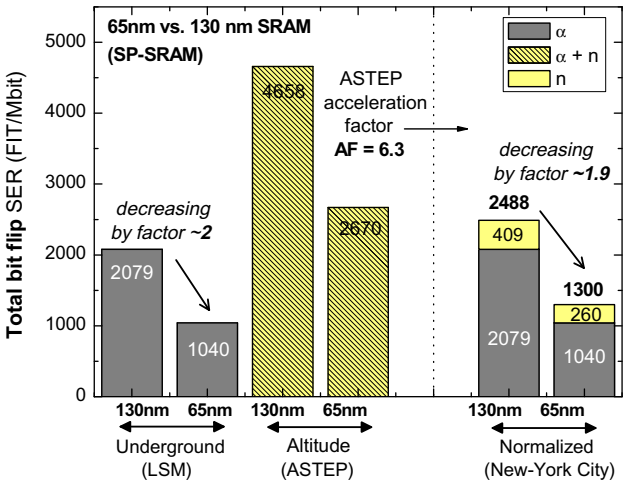

Fig. 8. Synthesis of experimental real-time SER values obtained for both 130 nm and 65 nm SP-SRAM from altitude and underground experiments and normalization of the SER at the reference flux of New-York City (sea-level) [18] taking into account: (i) the alpha contribution for the altitude test (fixed to the value measured at LSM) and (ii) the ASTEP acceleration factor AF = 6.3 for the neutron flux in altitude (experimentally measured using the Plateau de Bure neutron monitor).

the same order of magnitude the reduction of the alpha-emitter contamination for the 65 nm technology with respect to the 130 nm one. The discrepancy between SER-based and direct counting measurements is acceptable with respect to the experimental uncertainties for the alpha counting, the SER testing and the sample-to-sample/lot-to-lot variations for the trace amounts of alpha contaminants. The extraction of the amount of radioactive impurities naturally present in the circuit materials and at the origin of such levels of alpha emission rate is detailed in the next section.

5. Modeling and simulation aspects

In this last section, we would like to summarize our recent methodology combining numerical simulation and experimental data presented in Section 4 to extract the concentration of alpha-particle emitters present in the circuit materials and responsible of both the alpha-SER electrically detected on SRAM circuits and the alpha emission rate characterized using a gas flow type counter. This new method is illustrated here for the 130 nm technology; first results concerning 65 nm chips will be finally reported.

5.1. Monte-Carlo simulation of the alpha-SER

To evaluate the SER due to alpha-emitter isotopes contained in IC materials, we make the assumption of a predominant contribution of uranium contamination [5,37,38]. Uranium is naturally present in all terrestrial materials and is mainly composed of ^{238}U at 99.3%: its disintegration chain is composed of 14 daughter nuclei with eight alpha-emitters. Energies of the emitted alpha-particle are ranging from 4.20 to 7.68 MeV [39]; their corresponding ranges in silicon vary from 19 to 46 μm and their initial Linear Energy Transfer (LET) from 0.47 to 0.68 MeV/(mg/cm^2). All these values are detailed in Table 3. Note that the maximum LET reached by the emitted alphas is 1.45 MeV/(mg/cm^2) at Bragg's peak condition. Considering the uranium chain at the secular equilibrium, this signifies that all elements of the chain have the same activity. For a contaminated wafer with 1 ppb of uranium, this activity is equal to A_{Si} = 243.8 Bq/m^3 of silicon.

For the alpha-SER simulation, we consider a portion of the SRAM circuit composed of only silicon (see Fig. 9 up). Alpha-particle energy and track (starting point, unit direction vector) are randomly generated into the simulation volume for the eight alpha-emitters of the ^{238}U disintegration chain. As a function of

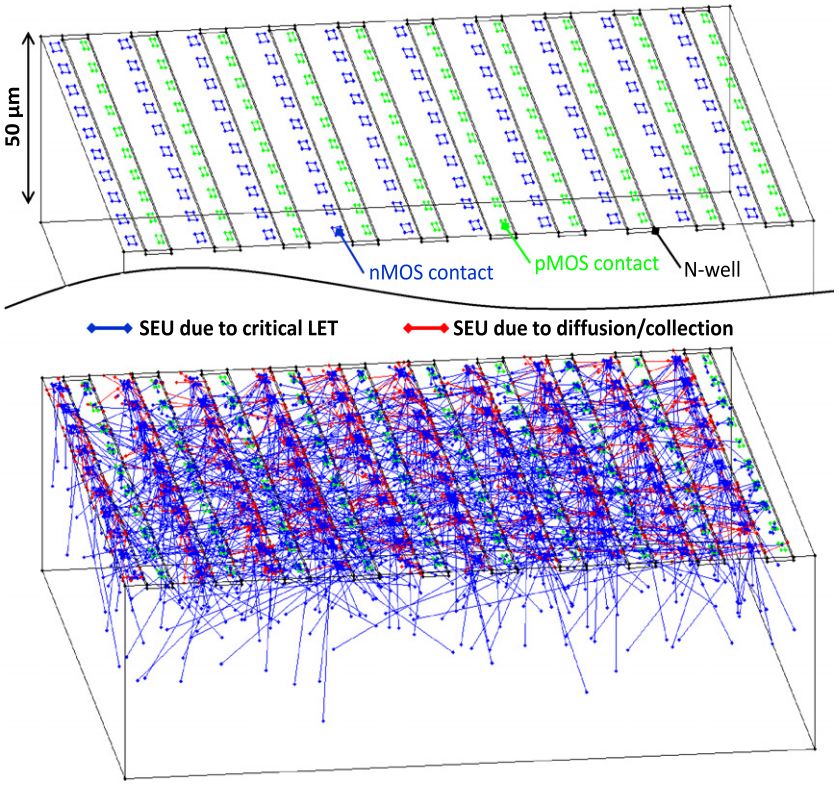

Fig. 9. Layout (up) and simulation result (down) of a 10 × 10 SRAM block. Blue segments (respectively red) represent alpha-particle tracks given a SEU due to critical LET (respectively due to diffusion–collection). In this example, a total of 100,000 alpha-particles have been generated for each nuclei of the decay chain. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Table 3
The alpha-particle emitters of the disintegration chain of ^{238}U.

	$T_{1/2}$ (s)	Alpha energy (MeV)	Range in Si (f)	Corresponding initial LET (MeV/(mg/cm^2))
^{238}U	$1.40 \times 10^{+17}$	4.19	18.95	0.677
^{234}U	$7.76 \times 10^{+12}$	4.68	22.17	0.634
^{230}Th	$2.38 \times 10^{+12}$	4.58	21.49	0.642
^{226}Ra	$5.05 \times 10^{+10}$	4.77	22.78	0.627
^{222}Rn	$3.30 \times 10^{+05}$	5.49	27.94	0.575
^{218}Po	$1.86 \times 10^{+02}$	6.00	31.86	0.545
^{214}Po	1	7.68	46.22	0.468
	64×10^{-04}			
^{210}Po	$1.20 \times 10^{+07}$	5.31	26.61	0.588

particle energy, the corresponding track length and LET is determined using tabulated SRIM tables [40]. Carriers generated along the track are discretized into punctual carrier density and their behavior can be considered to be governed by a pure spherical diffusion (with an ambipolar diffusion coefficient D) [41]. The final current transient extracted from a given contact (off-state drain) is obtained by integrating the product [diffusing charge × average collection velocity v] (evaluated at the level of the surface element $dx \times dy$) over the entire collection area [42]. The upset criterion for a particle track not crossing the drain junction is the $I_{max}T_{max}$ criterion. In the other case (track impacting the drain area), a critical LET criterion is chosen [43]. Parameters D, v, $I_{max}T_{max}$ and critical LET are technology dependent and have been obtained from TCAD and Spice simulation for the present 130 nm SRAM technology [44].

Fig. 9 (down) shows an example of simulation on a 130 nm SRAM block composed of 10 × 10 memory cells. In this example, a total of 100,000 alpha-particles has been generated for each radio nuclei of the decay chain in the simulation volume of 50 μm thickness (greater than the maximum range given in Table 3) with the LET and ranges corresponding to the eight alpha-emitters of the ^{238}U disintegration chain (same probability). Blue segments represent alpha-particle tracks that induced a SEU via the critical LET criterion; red ones correspond to particle tracks treated with the diffusion–collection model and leading to a SEU with the $I_{max}T_{max}$ criterion. In order to totally neglect border effects on the simulation volume considered, final results have been obtained for a larger SRAM block composed of 100 × 100 memory cells (20,000 sensitive contacts) with a total of 300,000 alpha-particles per radionuclei (total of 2.4×10^6 particles simulated). This large simulation shows that 0.6% of the generated alpha-particle tracks effectively lead to a triggered SEU. This result will be used in Section 5.2 to evaluate the contamination level of the circuits under test.

5.2. Extraction of alpha-particle emitter concentration from experimental alpha-SER

Considering that the soft-error rate measured underground is only due to the contribution (i.e. the activity) of alpha-particle emitters present in the circuit materials, our objective is to determine the level of radioactive impurity contamination leading to the time distribution of error shown in Fig. 7 (130 nm underground). From result of Section 5.2 (0.6% of the generated alpha-particles lead to a triggered SEU), we can easily evaluate the number N of SEU detected after T_{exp} hours for a real-time experiment involving M circuits:

$$N = [8 \times A_{Si} \times T_{exp} \times M \times S_{Cut} \times h] \times F \times 0.6\% \times X \,(\text{ppb}) \qquad (3)$$

where $8 \times A_{Si} = 1950$ Bq/m^3 corresponds to the total activity of the contaminated wafer for 1 ppb contamination, S_{Cut} is the surface of the 4 Mbit cut on the circuit for the 130 nm SRAM (10.48 mm^2), h is the thickness of the simulated silicon layer (50 μm), F is an alpha emissivity correction factor taking into account the difference in geometry between the simulated circuit and the real chip ($F = 0.99$, negligible in the present case due to a large and thick simulation volume considered), $T_{exp} = 22{,}720$ h, $M = 868$ chips and $N = 164$ SEU (see Table 2). The term into brackets in Eq. (3) corresponds to the total of alpha-particles emitted in the circuits during the measurement period. The only unknown value remains the real contamination level X of the chips (in ppb), which can be immediately determined to:

$$X = \frac{N}{[8 \times A_{Si} \times T_{exp} \times M \times S_{Cut} \times h] \times F \times 0.6\%} \approx 0.37 \text{ ppb} \qquad (4)$$

This value confirms an "ultra-low alpha" grade of the circuit materials, but also shows that such a very low contamination level leads to SEU that can be detected and quantified via underground tests. Considering now three different values $X = 0.2$, 0.37 and 0.5 ppb for this contamination level and calculating, in each case, the time scale for different Monte-Carlo simulation runs allows us to plot the corresponding simulated error distributions versus time on Fig. 10. We see that the bundle of curves computed with $X = 0.37$ ppb is perfectly superimposed to the experimental data, thus confirming the value of contamination previously extracted. Fig. 10 also shows that the confrontation of both computed and experimental data allows the extraction of X with a sub-0.1 ppb sensitivity.

A similar analysis based on the confrontation of experimental data and Monte-Carlo simulation for the 65 nm technology leads to an estimation of the contamination level of the chips equal to $X = 0.26$ ppb, evidencing a 1.4 reduction factor for this technology with respect to the 130 nm one.

5.3. Alpha-emissivity of circuit material (silicon)

In this last paragraph, we examine the alpha-particle emissivity from experimental and simulation viewpoints in order to verify if the contamination value extracted from the simulation of the real-time experiment is in agreement with wafer-level characterization (Section 4.3) and simulation of the alpha-particle emissivity. To compute such an emissivity, we simulated the spectra of alpha-particle escaping from the top face of 1 cm^2 layer of silicon (thickness 50 μm). A total of 100,000 alpha-particles have been generated in the Monte-Carlo code. If we consider a gas flow type detector similar to the instrument used for the wafer-level characterization located just in front of the top face (with a typical threshold value of 1.5 MeV for the detection of the escaping particles), our simulation shows that 13% of the total amount of particles generated in the bulk layer is detected. The alpha-particle layer emissivity E_α can thus be expressed as E_α (alpha/cm^2/h) = $0.13 \times 8 \times A_{Si} \times t_{Si}$, where $A_{Si} = 0.878$ (cm^3 h)$^{-1}$ is the activity of 1 ppb of ^{238}U in silicon, the factor eight counts for the eight alpha-emitters of the disintegration chain at secular equilibrium and $t_{Si} = 50$ μm is the silicon thickness. In this case, we obtain an alpha-particle emission rate of 4.56×10^{-3} alpha/cm^2/h, in excellent agreement with Ref. [38]. From this result, we can immediately conclude that the values of 1.1 and 2.3×10^{-3} alpha/cm^2/h experimentally measured respectively correspond to $1.1/4.56 \times 1$ ppb ≈ 0.24 and 0.5 ppb of uranium in the silicon wafer of the 130 nm SRAMs. This value interval is in good agreement with the value deduced from the previous extraction (0.37 ppb) combining the result of real-time experiment and Monte-Carlo simulation. The discrepancy between the different estimations is small and very acceptable with respect to the experimental uncertainties for the alpha counting, the SER testing and the sample-to-sample/lot-to-lot variations for

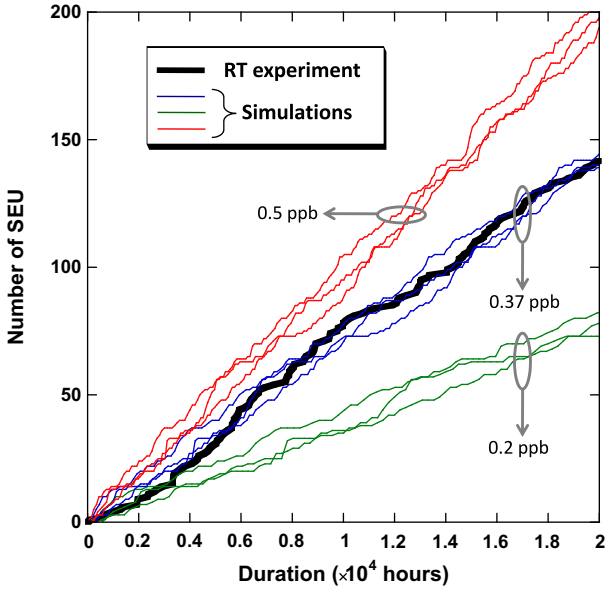

Fig. 10. Cumulative number of SEU versus test duration for the underground SER experiment (bold line). Several error distributions (thin lines) computed by Monte-Carlo simulations for different contaminations levels (0.2, 0.37 and 0.5 ppb of ^{238}U) are superimposed.

the trace amounts of alpha contaminants. We can conclude that both experimental data and numerical simulations converge towards the same value of uranium contamination, concordantly evaluated to a fraction of ppb in the range [0.2–0.5] ppb for this 130 nm SRAM technology. For the 65 nm technology and in a similar way, the value of $(0.9 \pm 0.3) \times 10^{-3}$ alpha/cm^2/h experimentally measured thus corresponds to $0.9/4.56 \times 1$ ppb $\approx$ 0.2 ppb of uranium in the silicon material, in excellent agreement with the value (0.26 ppb) previously extracted from the fitting of Monte-Carlo data on real-time SER measurements. These results demonstrate that the combination of experimental data and numerical simulations for both SER experiments and alpha-particle emissivity measurements is certainly a promising method to extract the contamination level of circuit materials in the sub-ppb range of atomic concentration with a good coherence between characterization at circuit and material levels within uncertainty margins. Future work will be conducted to consolidate and extend this approach for deca–nanometer technologies.

6. Conclusion

In summary, this paper presented a complete study dedicated to the soft-error rate characterization of CMOS SRAM memories in both altitude and underground environments. The different experiments have been conducted since 2005 on the ASTEP and LSM platforms, two permanent research installations (with specific instrumentation for the radiation environment characterization) dedicated to the evaluation of the impact of natural terrestrial radiation on the reliability of microelectronics circuits. Neutron and alpha-particle SER values, extracted from long duration real-time measurements, have been compared with data obtained from accelerated and wafer-level tests for two different (130 nm and 65 nm) technology nodes. The combination of these different tests allowed us to separate the SER component induced by atmospheric neutrons from that caused by on-chip alpha-particle emitters. In the particular case of the present tested SRAMs, this later is found to be five times larger than the neutron contribution at sea-level. Our data also clearly shows and quantifies via real-time experiments in natural environment the growing importance of MCU mechanisms when considering deep submicron technologies. Finally, this study highlights the importance of combining real-time measurements, accelerated tests, alpha emission characterization and numerical simulations to accurately estimate the soft-error rate of a given technology and the level of radioactive contamination in circuit materials. Such a multi-characterization approach should ensure that the different extracted values are consistent with the underlying calculation hypothesis and are within experimental error margins. Future works, currently in development, will continue on the ASTEP and LSM platforms in the following next years: they concern in particular the real-time characterization of 40 nm and 28 nm CMOS SRAM technologies, the installation of a permanent muon counter and a neutron spectrometer on the ASTEP platform.

Acknowledgements

This work is currently supported by the CATRENE Project # CA303 OPTIMISE (OPTImisation of MItigations for Soft, firm and hard Errors) and by the French Ministry of Economy, Industry and Employment under research convention #092930487. It previously benefited of support in part by the MEDEA+ Project #2A704 ROBIN, the Institut Carnot STAR (Marseille) and by the French Ministry of Economy, Finances and Industry under research conventions #052930215 and #062930210. The authors would like to thank D. Gautier and M. Derbey for their contribution to this work and the LSM staff for his efficient technical assistance. The logistical support of the Institute for Radioastronomy at Millimeter Wavelengths (IRAM) is also gratefully acknowledged. Special thanks are finally due to B. Gautier for his logistical support.

References

[1] Ziegler JF, Puchner H. SER – history, trends and challenges, cypress semiconductor; 2004 [see also references therein].
[2] O'Gorman TJ, Ross JM, Taber AH, Ziegler JF, Muhlfeld HP, Montrose ICJ, et al. Field testing for cosmic ray soft errors in semiconductor memories. IBM J Res Dev 1996;40(1):41–50.
[3] Leray JL. Effects of atmospheric neutrons on devices, at sea level and in avionics embedded systems. Microelectron Reliab 2007;47(9–11):1827–35.
[4] Dodd PE. Device simulation of charge collection and single-event upset. IEEE Trans Nucl Sci 1996;NS-43(2):561–74.
[5] Baumann RC. Radiation-induced soft errors in advanced semiconductor technologies. IEEE Trans Dev Mater Reliab 2005;5(3):305–16.
[6] Heidel DF, Marshall PW, LaBel KA, Schwank JR, Rodbell KP, Hakey MC, et al. Low energy proton single-event-upset test results on 65 nm SOI SRAM. IEEE Trans Nucl Sci 2008;55(6):3394–400.
[7] Dicello JF, McCabe CW, Doss JD, Paciotti M. The relative efficiency of soft-error induction in 4 K static RAMs by muons and pions. IEEE Trans Nucl Sci 1983;30(6):4613–6.
[8] Gelderloos CJ, Peterson RJ, Nelson ME, Ziegler JF. Pion-induced soft upsets in 16 M bit DRAM chips. IEEE Trans Nucl Sci 1997;44(6):2237–42.
[9] Duzellier S, Falguère D, Tverskoy M, Ivanov E, Dufayel R, Calvet M-C. SEU induced by pions in memories from different generations. IEEE Trans Nucl Sci 2001;48(6):1960–5.
[10] Roche P. Year-in-review on radiation-induced soft-error rate, tutorial at IEEE international reliability physics symposium. San Jose, USA; March 2006.
[11] Mitra S, Sanda P, Seifert N. Soft errors: technology trends, system effects and protection techniques. IEEE VLSI test symposium; 2008.
[12] Autran JL, Roche P, Borel J, Sudre C, Castellani-Coulié K, Munteanu D, et al. Altitude SEE test European platform (ASTEP) and first results in CMOS 130 nm SRAM. IEEE Trans Nucl Sci 2007;54(4):1002–9. <www.astep.eu>.
[13] Autran JL, Roche P, Gasiot G, Parrassin T, Schoellkopf JP, Borel J. Real-time soft-error rate testing of semiconductor memories on the European test platform ASTEP. In: Proceedings of the 2nd international conference on memory technology and design (ICMTD 2007). Giens, France; 7–10 mai 2007. p. 161–4.
[14] Autran JL, Roche P, Sauze S, Gasiot G, Munteanu D, Loaiza P, et al. Real-time neutron and alpha soft-error rate testing of CMOS 130 nm SRAM: altitude versus underground measurements. In: IEEE proceedings of the international conference on IC design and technology. Grenoble, France; June 2–4, 2008.
[15] Autran JL, Roche P, Sauze S, Gasiot G, Munteanu D, Loaiza P, et al. Altitude and underground real-time SER characterization of CMOS 65 nm SRAM. IEEE Trans Nucl Sci 2009;56(4):2258–66.
[16] Martinie S, Uznanski S, Autran JL, Roche P, Gasiot G, Munteanu D, et al. Alpha-emitter induced soft-errors in CMOS 130 nm SRAM: real-time underground

experiment and Monte-Carlo simulation. In: IEEE international conference on IC design and technology (ICICTD'10). Grenoble, France; June 2–4, 2010.
[17] Autran JL, Uznanski S, Martinie S, Roche P, Gasiot G, Munteanu D. A GPU/CUDA implementation of the collection–diffusion model to compute SER of large area and complex circuits. In: IEEE international conference on IC design and technology (ICICTD'10). Grenoble, France; June 2–4, 2010.
[18] JEDEC standard measurement and reporting of alpha particles and terrestrial cosmic ray-induced soft errors in semiconductor devices. JESD89 Arlington, VA: JEDEC solid state technology association. <http://www.jedec.org/download/search/JESD89A.pdf>.
[19] Stoker PH, Dorman LI, Clem JM. Neutron monitor design improvements. Space Sci Rev 2000;93:361–80.
[20] Clem JM, Dorman LI. Neutron monitor response functions. Space Sci Rev 2000;93:335–59.
[21] Dorman LI. Cosmic rays in the Earth's atmosphere and underground. Kluwer Academic Publishers; 2004 [chapter 6].
[22] http://www.seutest.com/FluxCalculation.htm.
[23] Lei F, Clucas S, Dyer C, Truscott P. An atmospheric radiation model based on response matrices generated by detailed Monte-Carlo simulations of cosmic ray interactions. IEEE Trans Nucl Sci 2004;51:3442–51.
[24] Lei F, Hands A, Clucas S, Dyer C, Truscott P. Improvement to and validations of the qinetiq atmospheric radiation model (QARM). IEEE Trans Nucl Sci 2006:1851–8.
[25] LSM. <http://www-lsm.in2p3.fr/>.
[26] Chazal V, Brissot R, Cavaignac JF, Chambon B, De Jésus M, Drain D, et al. Neutron background measurements in the underground laboratory of Modane. Astropart Phys 1998;9:163–72.
[27] Yakushev E. Neutron flux measurements in the LSM, LSM internal report. <http://www-lsm.in2p3.fr>.
[28] Lemrani R, Robinson M, Kudryavtsev VA, De Jesus M, Gerbier G, Spooner NJC. Low energy neutron propagation in MCNPX and GEANT4. arXiv:/arXiv:hep-ex/0601030v1.
[29] Baumann RC, Hossain T, Murata S, Kitagawa H. Boron compounds as a dominant source of alpha particles in semiconductor devices. Proc IEEE Int Reliab Phys Symp (IRPS) 1995;297–302:1995.
[30] Baumann RC, Smith EB. Neutron-induced boron fission as a major source of soft errors in deep submicron SRAM devices. Proc IEEE Int Reliab Phys Symp 2000;10:152–7.
[31] http://www.synopsys.com/products/tcad/tcad.html.
[32] Gasiot G et al. Alpha-induced multiple cell upsets in standard and radiation hardened SRAMs manufactured in a 65 nm CMOS technology. IEEE Trans Nucl Sci 2006;53(6):3479–86. Part 1.
[33] Gasiot G, Giot D, Roche P. Multiple cell upsets as the key contribution to the total SER of 65 nm CMOS SRAMs and its dependence on well engineering. IEEE Trans Nucl Sci 2006;54(6):3479–86. Part 1.
[34] Giot D, Roche P, Gasiot G, Autran J-L, Harboe-Sørensen R. Ion testing and 3D simulations of multiple cell upset in 65 nm standard SRAMs. IEEE Trans Nucl Sci 2008;55(4):2048–54.
[35] iRoC Technologies. <http://www.iroctech.com/sol_test_112.html>.
[36] Kobayashi H, Usuki H, Shiraishi K, Tsuchiya H, Kawamoto N, Merchant G, et al. Comparison between neutron-induced system-SER and accelerated-SER in SRAMs. Proc IEEE Int Reliab Phys Symp. Phoenix, USA; 2004. p. 288–93.
[37] Wrobel F, Gasiot J, Saigné F. Hafnium and uranium contributions to soft-error rate at ground level. IEEE Trans Nucl Sci 2008;55(6):3141–5.
[38] Wrobel F, Saigné F, Gedion M, Gasiot J, Schrimpf RD. Radioactive nuclei induced soft errors at ground level. IEEE Trans Nucl Sci 2009;56(6):3437–41.
[39] Adamiec G, Aitken M. Dose-rate conversion factors: update. Ancient TL 1998;16(2):37–50.
[40] SRIM software. <http://www.srim.org/>.
[41] Palau JM, Hubert G, Coulié K, Sagnes B, Calvet MC, Fourtine S. Device simulation study of the SEU sensitivity of SRAMs to internal ion tracks generated by nuclear reactions. IEEE Trans Nucl Sci 2001;48(2):225–31.
[42] Hubert G, Bougerol A, Miller F, Buard N, Anghel L, Carriere T, et al. Prediction of transient induced by neutron/proton in CMOS combinational logic cells. In: Proceedings of the 12th IEEE international on-line testing symposium (IOLTS'06).
[43] Munteanu D, Autran JL. Modeling of digital devices and ICs submitted to transient irradiations. IEEE Trans Nucl Sci 2008;55(4):1854–78.
[44] Correas V. Prédiction de la section efficace des aléas logiques (SEU) e du taux d'aléas multiples (MCU) de technologies CMOS déca-nanométriques sous irradiation aux ions lourds. Thèse de Doctorat, Université Montpellier II; 2008.