Journal of Manufacturing Processes 32 (2018) 222–229

Contents lists available at ScienceDirect

Journal of Manufacturing Processes

journal homepage: www.elsevier.com/locate/manpro

Technical Paper

Multilevel process on large area wafers for nanoscale devices

B.J. Pires[a,1], A.V. Silva[a,b], A. Moskaltsova[a,2], F.L. Deepak[c], P. Brogueira[b,d], D.C. Leitao[a,b,*], S. Cardoso[a,b]

[a] INESC – Microsystems and Nanotechnologies (INESC-MN) and IN, Rua Alves Redol 9, 1000-029 Lisboa, Portugal
[b] Instituto Superior Tecnico (IST), Universidade de Lisboa, Av. Rovisco Pais, 1049-001 Lisboa, Portugal
[c] Department of Advanced Electron Microscopy, Imaging and Spectroscopy, International Iberian Nanotechnology Laboratory (INL), Av. Mestre Jose Veiga, Braga 4715-330, Portugal
[d] CeFEMA, Instituto Superior Tecnico (IST), Universidade de Lisboa, Av. Rovisco Pais, 1049-001 Lisboa, Portugal

ARTICLE INFO

Article history:
Received 11 September 2017
Received in revised form 25 January 2018
Accepted 26 January 2018
Available online 20 March 2018

Keywords:
Nanofabrication
Electron beam lithography
Reactive ion etching
Metrology

ABSTRACT

Spintronic nanodevices are consolidating a highly reputed position in advanced manufacturing industry, not only due to progresses in magnetic hard disk sensors, but also the memory market. The ability to integrate magnetic thin films on large area wafers and subsequent nanofabrication into functional devices is key for such success. This work describes methodologies used for definition of sub-100 nm pillars, using reliable via opening to contact nanopillars buried in a dielectric film. A two consecutive step electron beam lithography process is used to fabricate current-perpendicular-to plane nanodevices. The first step is required to pattern nanopillars down to 30 nm. The second provides access to nanopillar top through nanovias definition and reactive ion etching. Optimum alignment of multilevel exposures ensures the most accurate positioning in the shortest time. Most importantly, the results are obtained on 150 mm diameter wafers, where additional challenges of uniformity of resists, oxides and metals are critical for end-point control and improved yield of fabricated devices. The design of customized test structures allowed control of etching end-point.

1. Introduction

The semiconductor industry drives the metrology settings and nanofabrication standards in electronic device manufacturing. Given the reality of globalized markets, the massive production nodes of the semiconductor industry offer advanced manufacturing capabilities for other technologies, seeking a nanoelectronic capability extension [1,2]. One such example is spintronics, where the semiconductor industry could offer additional electronic functionalities, enabling nanofabrication of monolithic devices (e.g. MRAM, oscillators or read heads) by using compatible processing tools. Therefore an explosive growth in production capability for such devices requires manufacturing over large area wafers with large yield of functional structures. As industry maintains a high degree of confidentiality, the challenges in integrating and matching nanofabrication processes at distinct patterning levels is mostly overlooked in literature. Research groups working on spintronics have been consolidating advanced deposition, nanopatterning and metrology [3,4], compatible with large area wafers [5–7]. Although few reports exist on successful processes carried out by industry [7–9], many technical achievements remain not available in scientific publications.

Two of the challenging points across the spintronic nanodevice fabrication in 150 mm wafers are definition of sub 100 nm pillars and nanovia access to them. Lift-off has been employed in 25 mm substrates achieving magnetic tunnel junctions (MTJ) $\geqslant$100 nm [10]. Chemical mechanical polishing (CMP) reduces process time (compared to liftoff) [11,12,5] but requires a tight control of the end-point. Ion beam dry planarization has also been used [13], as do self-aligned methods although requiring careful matching between photoresist thickness and oxide etching rates, together with a controlled reactive ion etching (RIE) uniformity [14]. A broad view of the challenges and strategies used for magnetic device nanopatterning can be found in reference [3].

The strategy described here includes a two-step electron beam lithography (EBL), combined with nanovia opening using RIE. The alignment of multilevel features using optical lithography and EBL is optimized to ensure the most accurate positioning in the short-

* Corresponding author at: INESC – Microsystems and Nanotechnologies (INESC-MN) and IN, Rua Alves Redol 9, 1000-029 Lisboa, Portugal.
[1] Presently at International Iberian Nanotechnology Laboratory (INL), Av. Mestre Jose Veiga, Braga 4715-330, Portugal.
[2] Presently at Center for Spinelectronic Materials and Devices, Department of Physics, Bielefeld University, Universitätsstraße 25, 33615 Bielefeld, Germany.

https://doi.org/10.1016/j.jmapro.2018.01.024
1526-6125/

est exposure time. Furthermore, this study is performed in large area wafers where additional challenges regarding uniformity of resist layers, oxide films and metallic thin films, over the whole surface area, are critical for an improved yield of fabricated devices. These methodologies are somehow followed by the semiconductor industry, however the particularity of spintronic devices laid on ultrathin films (e.g. 1 nm critical thickness for the MTJ tunnel barrier, thin dielectric layers, thin resist thickness), imposes very narrow tolerances for the etching end-point control. The inclusion of customized test structures allowed to control the RIE end-point. As a result, we demonstrate a controlled nanofabrication process that can be followed in pre-production stages, shortening the path from innovative spintronic materials and devices to a large scale manufacturing level in a semiconductor-compatible foundry facility.

2. Results and discussion

Fig. 1 illustrates the main fabrication steps. The optimization of the proposed nano-process includes: (i) exposure of the nanovias by EBL critically aligned over nanopillar buried in oxide and (ii) accurate control of the RIE end-point for opening vias. Monitoring of deposition and etching uniformity during this step is key for a successful nanofabrication over the whole wafer area.

One starts by the deposition of the magnetic tunnel junction (MTJ) stack on a Nordiko 3000 ion beam deposition (IBD) tool. The used stack was based on the following structure: buffer/CoFeB/AlOx/CoFeB/cap, where the oxide barrier is 14 Åthick. The barrier oxidation was performed with remote plasma oxidation with a mixed Ar-O_2 plasma for 15 s after each 7 Å deposition of Al (pressure 0.6 mTorr, plasma voltage ≈15 V) [15]. A thick cap, usually Ta, is required as protective layer during RIE via opening. Ta provides a low etching rate and low material cost (compared with Pt, a highly selective alternative).

Bottom electrode (BE) is defined using optical lithography and Ar^+ ion milling at 70° (beam current 105 mA, ≈390 μA/cm^2 with +735 V; working pressure of 0.2 mTorr) [Fig. 1(B)].

2.1. Nanopillar definition

The wafer is then spin-coated with an electron sensitive negative resist whose thickness is critical to achieve EBL minimum size in the used tool (≈30 nm) [12]. A systematic study of spinning time, velocity, dispensed volume, and their impact on thickness (t_{avg}) and (non)uniformity (NU_{res}) was performed. Fig. 2(a) and (b) shows a representative t_{res} wafer map, from which we extract NU_{res}, calculated as $\frac{t_{max}-t_{min}}{2t_{avg}}$. Average resist thickness (t_{avg}) is calculated from 72 points uniformly distributed over the wafer, and its dependence on the spinning speed is depicted in Fig. 2(c). A decrease of t_{avg} to (87.0 ± 0.5) nm and NU_{res} to 1.1%, was obtained with increasing spinning speed up to 4 krpm. For spinning durations larger than 30 s, no significant uniformity improvement was observed. The optimized recipe was then used (spinning speed = 4 krpm during 30 s) followed by a bake at 85 °C for 60 s.

EBL is performed on a Raith-150 system using an acceleration voltage of 20 kV and aperture size of 10 μm, corresponding to beam currents ≈33 pA. Circular pillars were defined using the dot exposure mode. Fig. 3 displays the calibration curve for dot size versus dose, showing a linear dependence below 100 nm. For process validation a dot dose of 0.045 pC was used for a nominal dot diameter of 70 nm. The beam focal distance was controlled and corrected via software, to ensure well defined nanostructures along the entire wafer with size deviation from nominal of the order of 5%. This strategy showed an improvement on pillar maximum resolution

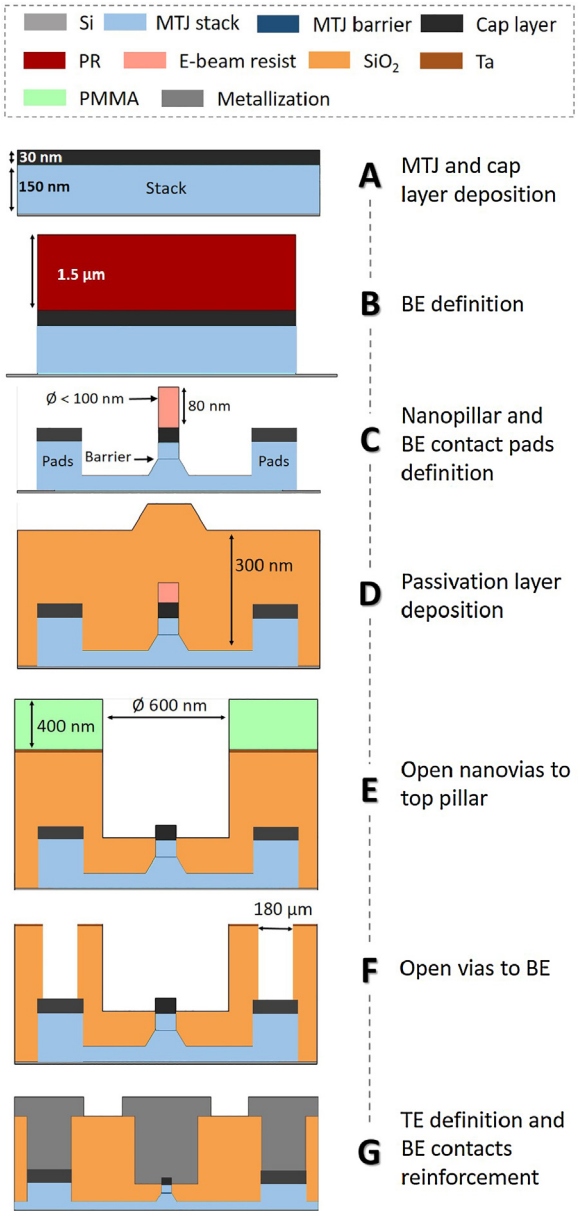

Fig. 1. Layout of the nanofabrication process: (A) MTJ and cap layer deposition, (B) BE definition by optical lithography and ion beam etching, (C) nanopillar and BE contact pads definition by EBL and two-step ion beam etching, (D) passivation layer deposition, (E) opening of the nanovias to top pillar contact, (F) opening of the vias to bottom pads using RIE and (G) TE definition and BE contact pads reinforcement by optical lithography and metallization. Schematics not to scale.

compared to area mode exposure, but with a strong dependence on stigmation correction and aperture alignment.

For long exposures, the stage drift relative to electron beam fixed position has also to be taken into account. According to Goodberlet et al., thermal effects and/or charging may be at the origin of the observed drift over time [16]. In this case, an incremental deviation will affect precision alignments such as via-to-pillar. Quantification was performed by scanning a cross-shaped mark every minute (up to 7h) and measuring its deviation relative to the center [Fig. 4(a)–(c)]. Fig. 4(d) shows all measurements overtime for both x and y directions. A plateau is visible over the first minutes upon loading the sample, starting to increase after ≈150 min. This difference is attributed to thermalization of the column and sample [16], and is consistent with information from manufacturer. Overall, a drift smaller than 3.5 nm/min is observed. Although for short

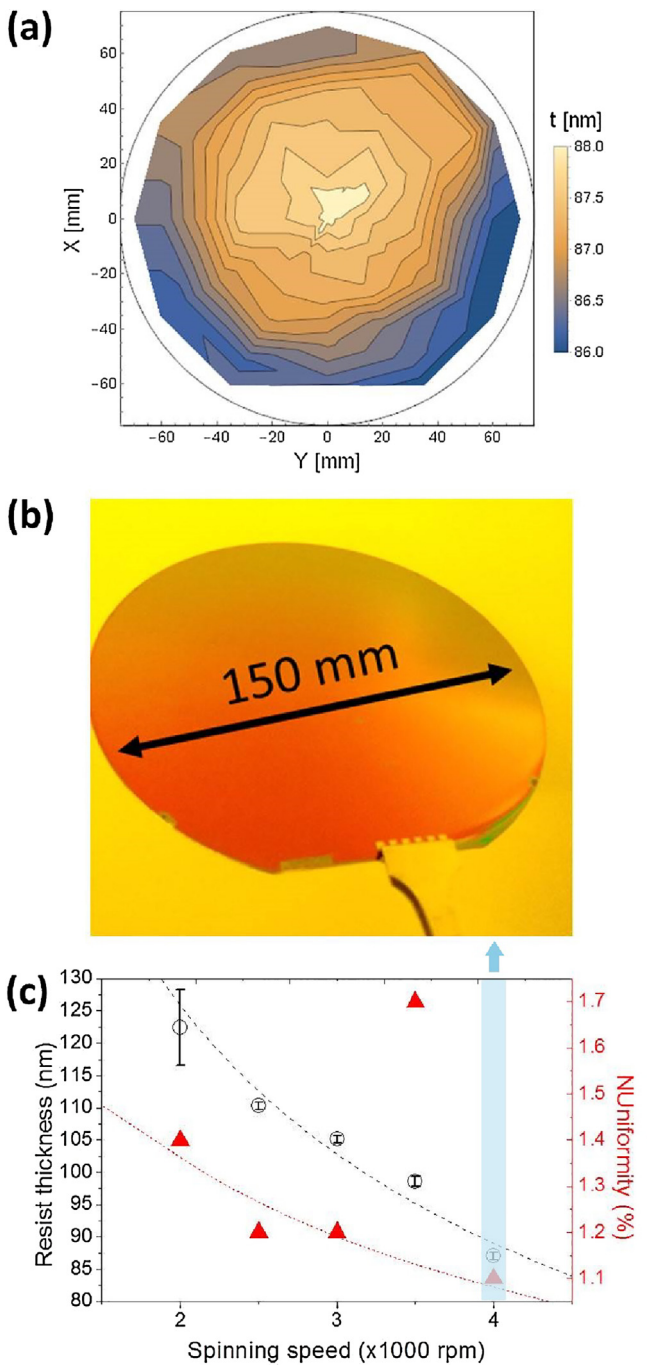

Fig. 2. Resist thickness optimization on 150 mm wafer for EBL:(a) representative wafer map of resist thickness (4 krpm for 30 s; 5 mL dispensed resist) using ellipsometry and (b) corresponding image highlighting the uniformity of the coating. (c) t_{avg} (obtained from a total of 72 points on the wafer) and coating NU_{res} dependence on the spinning speed. The spinning time was constant – 30 s.

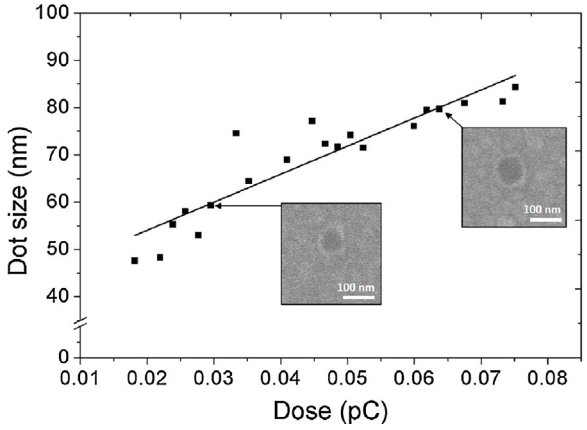

Fig. 3. Calibration of dot size versus dot dose. The insets show SEM images of selected circular shapes obtained using dot exposure mode.

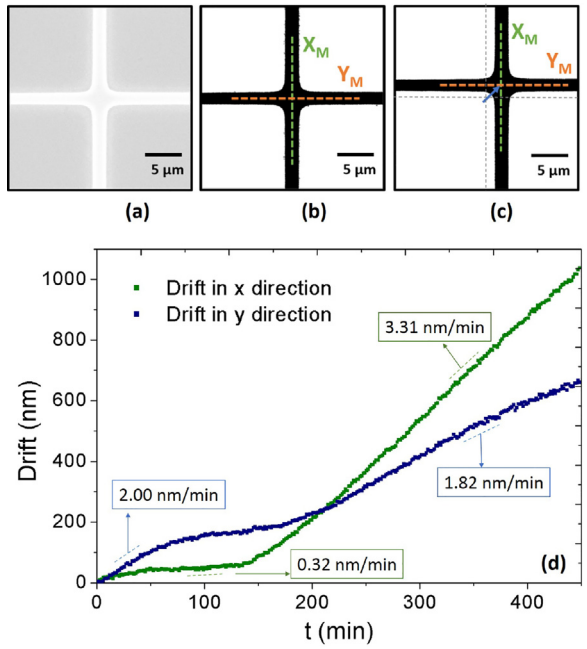

Fig. 4. Assessment of stage drift relative to the fixed electron-beam position. Illustration of the procedure used for drift analysis: (a) SEM image of the cross-shaped mark used in this study, (b) mark position recognition (at time = 0 s), and (c) mark position recognition time = 7 h. (d) Stage drift measurements over time.

exposure times and/or small areas this is not significant, in 1 h it can move ~210 nm, thus becoming a major factor when alignment precision below 200 nm is necessary.

The nano-pattern is then transferred to the underlying stack using a two-step ion milling etching [17,10,11]. Different strategies were reported, either involving conventional photo-lithography combined with ion beam etching to reduce the lateral size of the MTJ pillar down to 20 nm [18] or unconventional alternatives as nanosphere lithography [19]. More commonly, one can find nanopatterning using hard-masks and EBL on positive resist [18,20–22,5], or negative resist as mask [11,17,10]. Although RIE [21,18,5] or metal etcher techniques [23] can also be used to define the nanopillar, ion milling overcomes corrosion and oxidation, as reported by most RIE processes [24,25]. Also, this technique as the advantage of changeable average beam directionality, providing in the same run a vertical profile and a grazing angle for removal of redeposited material.

Here, a combination of Ar^+ beam at 70°, is used until the barrier to implement the vertical profile, followed by an etching angle of 40° [Fig. 1(c)]. This last step creates a tapered profile and reduces redeposition which affects the performance of the tunnel barrier device, even more critical for nano-sized dimensions [11]. Alternatives as oxygen showering have also been used to recover from redeposited materials at the sidewalls of very small MTJ devices [7].

2.1.1. Multilevel alignment and exposure time optimization

The exposure mask was divided into $20 \times 20\,mm^2$ dies [Fig. 5(a)], enclosing 1444 write-field (WF) areas of 500 µm. This

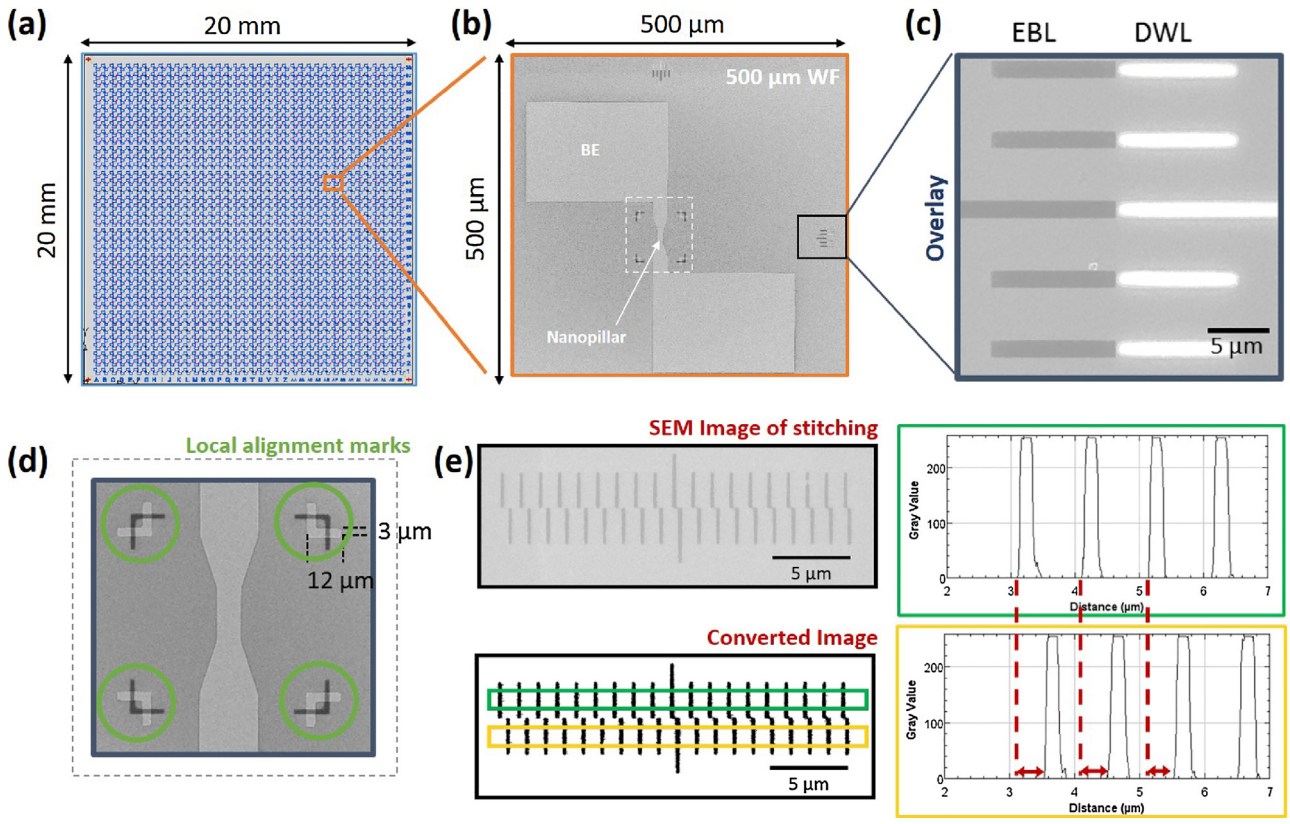

Fig. 5. Masks, structures layout and procedures for stitching error analysis. (a) Mask layout used within a die of $20 \times 20\,mm^2$. (b) Bottom electrode, nanopillar and set of nonius lines in each border of the WF = $500 \times 500\,\mu m^2$. (c) Nonius lines defined at different exposure levels, namely 1st level with bottom electrode definition and 2nd level EBL for nanopillar exposure. (d) Layout of the alignment marks design for automatic recognition using Raith 150 software. (e) Procedure for evaluation of deviations using image analysis: correct structures recognition and automatic deviation quantification.

arrangement ensures a reduced stage movement, decreasing exposure duration due to smaller stage/beam settling times. Drawbacks include defocusing at WF edges, enhanced stitching errors and loss of critical dimension control [26], being the latter mitigated by placing critical features within the WF middle, as seen in Fig. 5(b).

To automatically quantify the stitching errors and overlay performance in both directions, test structures such as nonius, were included at the WF borders [Fig. 5(b), (c) and (e)]. The stitching precision was first evaluated with consecutive EBLs leading to the pattern observed in Fig. 5(e). Scanning electron microscopy (SEM) image analysis for automatic edge detection enabled to quantify deviations between each pair of lines (top and bottom set of nonius). Finally, we obtained a stitching error of (322 ± 24) nm on the horizontal direction and (52 ± 12) nm on the vertical direction. Smaller errors of ≈33 nm were reported for a WF = 100 µm using the Raith 150 tool [16,27]. Here, the use of a WF = 500 µm requires a lower magnification at the column, leading to increased deviations in WF alignment [28].

The multilevel (mis)alignment was then evaluated between BE and nanopillar exposure (BE-to-pillar misalignment) [Fig. 5(b) and (c)]. Half of the nonius are patterned during BE definition with optical lithography, being the remainder half defined during EBL [Fig. 5(c)]. To correct sample-to-beam deviations we used the automatic mark recognition feature of the system, where in each WF the system scans 8 line-marks (4 in *x*-direction and 4 in *y*-direction) taking ~40 s [Fig. 5(d)]. To reduce the effective exposure time, which includes alignment plus feature definition, we have determined which reduced number of WF alignments yielded, at the same time, a small exposure time and accurate alignment. For that, we have measured in a full 150 mm wafer (28 dies of $20 \times 20\,mm^2$) the stitching error after performing auto-align in (i) all elements, (ii) each 2 elements, (iii) each 5 elements and (iv) each 10 elements. Table 1 summarizes the obtained results. A deviation reduction down to ≈202 nm was achieved while increasing the number of elements used for WF alignment, leading however to unbearable exposures times of to ≈2 weeks for 150 mm wafers. These results are larger than reported by other groups using the same system [16]. For our system, auto WF alignment correction in each five elements (2500 µm separation), minimizes stage drift to ≈3 nm, enabling a final accurate nanopillar exposure along the whole wafer, with optimized total exposure time of ≈3.5 days, without comprising BE-to-nanopillar positioning. Finally, this study enabled the minimization of non-functional structures, while providing the best time/accuracy trade-off.

2.2. Opening vias through the oxide to nanopillars

A thick 300 nm SiO_2 passivation layer is then deposited over the nanopillar to insulate side-walls and BE from top electrode [Fig. 1(D)]. Deposition was performed using plasma-enhanced chemical vapour technique (PECVD Delta Electrotech), and conditions were as follows, 2500 sccm of NO_2 and 125 sccm of SiH_4 with 430 W RF power, leading to a working pressure of 700 mTorr, and process temperature of 300 °C. Ellipsometry measurements over the entire wafer provided a (non)uniformity of NU = 6.0% [Fig. 6(a)-(b)]. Quantification of the thickness profile and RIE process enables an optimum control of end-point for the opening vias step. The wafer is then spin-coated with PMMA, an electron sensitive positive resist at 3 krpm during 30 s for a nominal thickness of 400 nm. Follows a bake at 160 °C for 4 min. The volume of dispensed resist is ~10 mL for each wafer. Nanovias with 600 nm diameter defined at mask level, are exposed with a dose of 150 $\mu C/cm^2$, accelera-

Table 1
EBL exposure time for a 150 mm wafer and misalignment results obtained for a different number of aligned WF.

	Auto-align in			
	All elements	Each 2 elements	Each 5 elements	Each 10 elements
Die exposure time	≈13 h	≈7 h	≈3 h	≈90 min
Wafer exposure time	≈2 weeks	≈1 week	≈3 days	≈1.5 day
BE-to-pillar misalignment (nm)	202	297	322	371
Pillar-to-vias misalignment (nm)	253	275	332	372

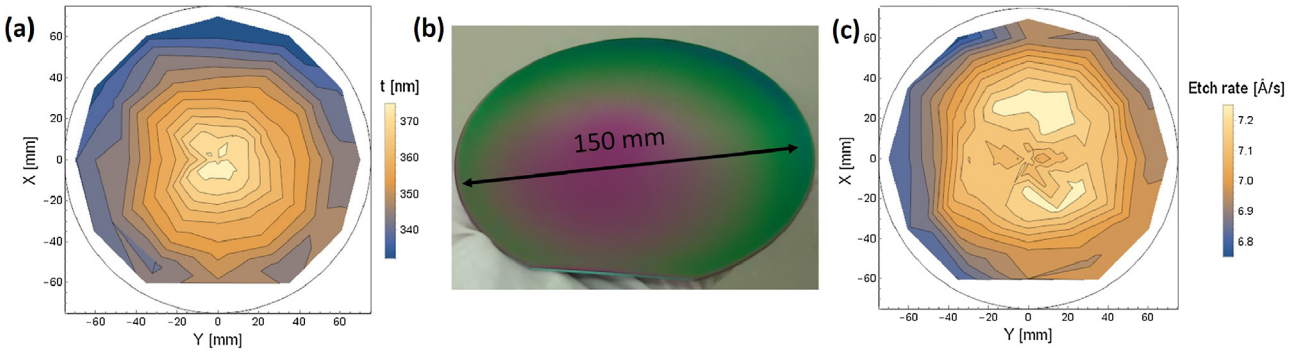

Fig. 6. (a) Map of SiO_2 thickness on a Si blank wafer, showing a NU=6.0% and (b) corresponding image where a color gradient correlates with the thickness profile. (c) RIE map of the SiO_2 wafer in (a) displaying a RIE NU=7.1%. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

tion voltage of 10 kV and aperture size of 10 μm, corresponding to beam currents ≈22 pA, as optimized elsewhere [29]. Sample is then developed for 80 s with AR 600-55 [Fig. 7(a)]. Profiting from the study described in Section 2.1.1, a tolerance of 300 nm corresponding to half of nominal diameter of the patterned nanovias was considered acceptable. From Table 1, the approach of aligning in each five WF elements was used, minimizing possible vias-to-pillar misalignments. The automatic mark recognition is performed, in distinct WF from those used in 1st EBL exposure, ensuring correct reading.

Fig. 7 shows SEM consecutive images corresponding to 6 adjacent WF with the via aligned over the nanopillar. Notice that only the first and last ones underwent auto-align procedure, but still an accurate vias-to-pillar definition was achieved within settled tolerance. This consecutive SEM images show a successful multi-level alignment, which supports the implemented methodology for

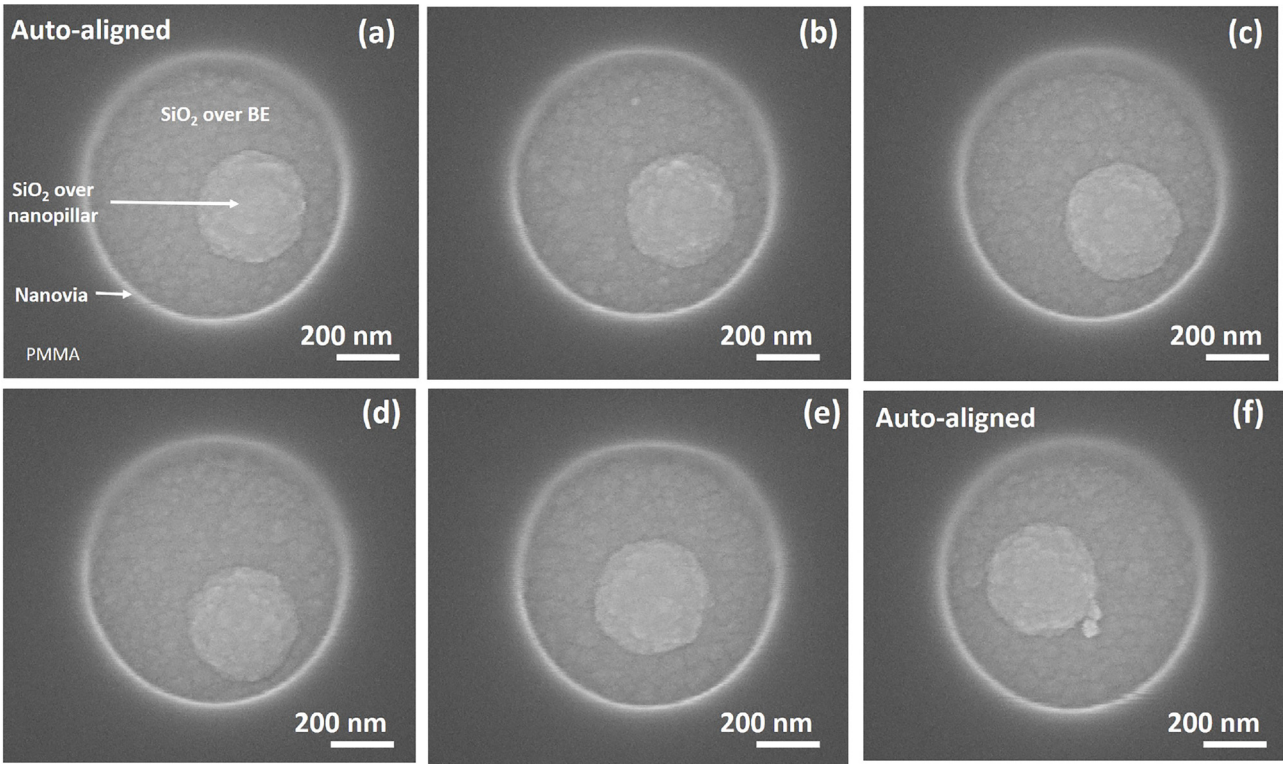

Fig. 7. Consecutive SEM images in 6 adjacent WF with via aligned over the nanopillar. After 5 elements, WF is auto-aligned with accurate vias-to-pillar deviation within settled tolerance.

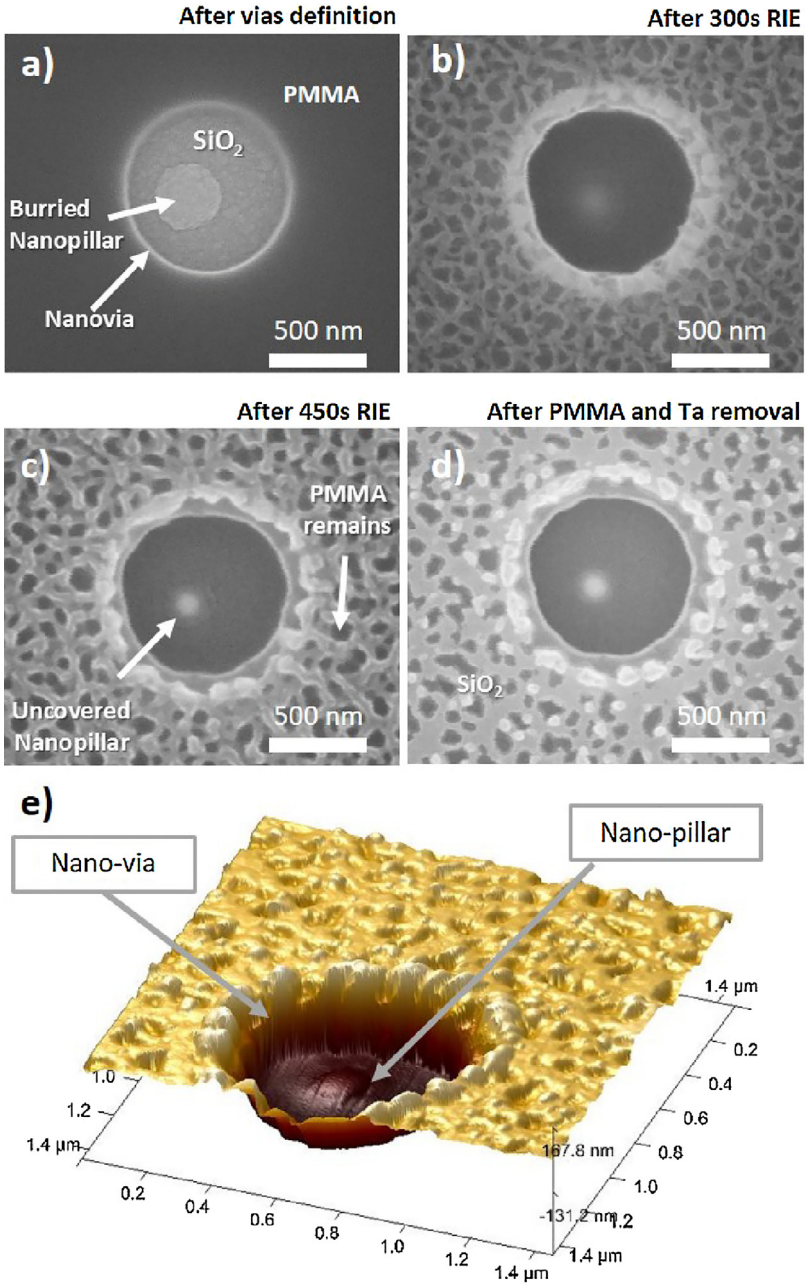

Fig. 8. Opening nanovias to top pillar step: SEM images after (a) nanovias EBL exposure on PMMA (≈600 nm lateral size), (b) and (c) RIE to top pillar until pillar is revealed, (d) PMMA and Ta removal with O_2 plasma and IBD. (e) AFM measurements around nanovia region, showing an over-etch depth around the MTJ pillar ≈35–50 nm.

exposure. A major challenge relates to the correct recognition of WF marks defined underneath the thick oxide (at the bottom electrode level; 1st lithography). Charging effects hinder marks recognition by the software, limiting the alignment yield to ≈90% in the entire wafer.

The SiO_2 is then removed by RIE (LAM Rainbow 4520 model) with 200 sccm of Ar and 100 sccm of CF_4 under a pressure of 140 mTorr. Ellipsometry measurements provided a RIE NU = 7.1% for SiO_2 with an etch rate ≈7 Å/s [Fig. 6]. To control the RIE end-point device-like test structures were included for SEM and AFM. SEM inspection was done at distinct RIE stages, until the top pillar was uncovered. Fig. 8(a) shows the nanopillar (through the PMMA via) covered by the passivation layer. After 300 s of RIE, one clearly sees a reduced bump over the nanopillar consistent with oxide removal [Fig. 8(b)]. Further increase in RIE time leads to a much brighter contrast, indicative of an uncovered nanopillar cap layer. Alongside, a change in the PMMA surface topography is also visible [Fig. 8(c)]. These features act as a mask for etching of SiO_2 outside the via, leading in the end to a similar pattern transferred to the top surface of SiO_2 [Fig. 8(d)]. Still, given the thickness of the oxide, such porosity does not affect the insulation of top to bottom electrodes.

AFM measurements in the center of the wafer, where the RIE and oxide thickness are more uniform [Fig. 8(e)], showed an etch depth of 38 nm below the cap layer (30 nm thick). This value increased to 49 nm at wafer borders. The etch depth values below cap layer suggest that oxide around the barrier was not removed as intended to ensure sidewall insulation. For these AFM experiments we used a D3100 with a Nanoscope IIIa controller from Digital Instruments (DI). The measurements were performed in tapping mode™ under ambient conditions. We used a commercial tapping mode etched

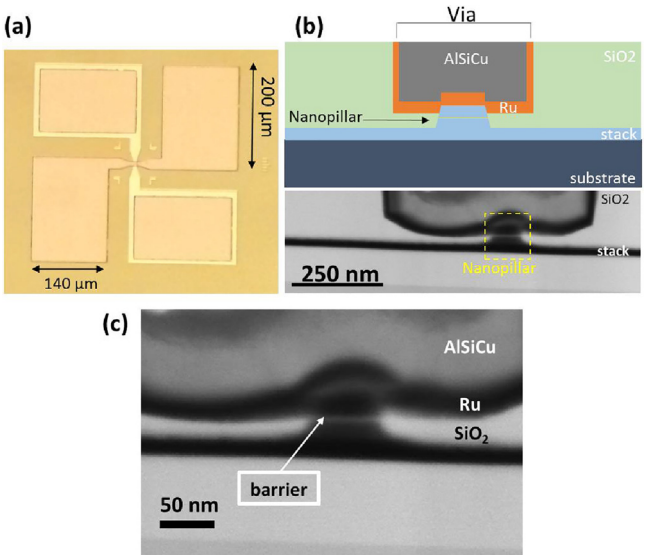

Fig. 9. (a) Top view of the final device. (b) FIB-SEM image of the nanopillar cross-section and corresponding labelling. (c) Detailed view over the nanopillar.

silicon probe from DI and a $90 \times 90\ \mu m^2$ scanner. Images consisted of raster scanned, electronic renderings of sample surfaces.

At the end, the remainder PMMA was removed with O_2 plasma (20 sccm of O_2, pressure of 275 mTorr) [Fig. 8(d)].

2.3. Final device

Finally, vias to bottom pads are defined by optical lithography and opened with RIE [Fig. 1(F)]. Then, top contact metallization and bottom contact reinforcement is performed in with Ru 40/AlSiCu 300/$TiWN_2$ 15 (values in nm). The first Ru layer is deposited by ion beam, ensuring a good step coverage of nanovia and of nanopillar top [10], providing a good wetting of the surface. Fig. 9(b) shows a FIB-SEM cross section image of a nanodevice, prepared using a focused ion beam (FIB – Helios NanoLab Dual Beam FIB-SEM) at 30 kV. The SEM cross section shows a conformal Ru layer coverage of the via sidewalls and nanopillar [Fig. 9(b)]. This is followed by sputtered AlSiCu/TiW and lift-off [Fig. 1(G)], showing a successful filling of the via [Fig. 9(b) and (c)]. The cross-sectional analysis also demonstrates that with the proposed method, we were able to remove the oxide over the pillar, while controlling the end-point of the RIE before reaching the MTJ barrier. This is critical to ensure that current flowing through the device crosses the top ferromagnetic electrode and then the insulating barriers. Only then a large change in signal will be observed. Furthermore, an accurate sidewall insulation of the nanopillar is achieved with SiO_2, and no significant porosity is observed in this layer, as discussed above.

2.4. Outlook

According to Lau et al. [3] accurate control of the magnetic properties in nanostrutures (e.g. coercive field value and distribution, anisotropy, demagnetizing fields) requires minimization of physical defects introduced during fabrication. A main source of edge defects and re-deposition arises during nanopillar definition usually done by etching techniques. We employ ion-milling to define the pillar, pointed as advantageous for nanostructuring when compared to RIE [24,25]. Our system also allows removal of redeposited material by changing the etching angle. This tappers the profile of the nanoelement, but is only done after patterning the free-layer with steep walls to ensure a correct magnetic behavior [30]. Due to lack of selectivity the thin resist mask used (80 nm) is partially removed during ion milling etching. A thick cap layer (Ta 30 nm), designed to protect MTJ during the RIE to open vias, also prevents ion-milling from damaging the stack.

A disadvantage of EBL is being very time consuming [3]. Our optimized alignment strategy was efficient in reducing significantly exposure duration while maintaining a high degree of positioning. In addition, the point-by-point control of the beam focus ensured minimal dispersion in feature size and shape, both critical to control the magnetic behaviour.

Finally, to individually characterize the magnetic nanodevices, most common local measurements focus on magneto-transport [4,18,10,13]. Conductive AFM has also been used [31] although no top metallic electrode is defined. We reported recently on well performant perpendicular MgO-MTJs for STT-MRAM. The nano-MTJs were fabricated using this methodology, and the mechanisms of breakdown were studied in detail [32].

3. Conclusions

We demonstrate a successful nanofabrication process based on two EBL exposures, ion beam milling and RIE. Our method shows reliable alignment on 150 mm wafers between 70 nm nanopillars and 600 nm nanovias. Major parameters of the EBL system were accessed thus improving and guaranteeing a high fabrication yield of magnetic nanodevices. Optimization of multilevel lithography alignment procedure ensured the shortest exposure time while delivering accurate placement of nanovia-over-nanopillar. Furthermore, using dedicated test structures we have also demonstrated a control of RIE end-point. This ensured that etching stopped at the top ferromagnetic layers, well above the extremely thin barrier. Full wafer inspection yielded ≈90% of well aligned nanovias/nanopillars supporting the proposed methodology for nanofabrication of magnetic current-perpendicular-to-plane devices.

Acknowledgements

Work partially supported by FCT-project PTDC/CTM-NAN/4737/2014, EXCL/CTM-NAN/0441/2012 and FP7-PEOPLE-2012-ITN-316657 (SPINICUR). D.C. Leitao acknowledges financial support through FSE/POPH. INESC-MN acknowledges funding through the Associated Laboratory IN. FLD acknowledges the financial support by the ERDF (ON.2 – O Novo NorteProgram).

References

[1] ITRS – International Technology Roadmap for Semiconductors www.itrs.net/reports.html.
[2] Guan Y, Tortonese M. Metrology standards for semiconductor manufacturing, vol. 1; 2004. p. 588–93.
[3] Lau JW, Shaw JM. Magnetic nanostructures for advanced technologies: fabrication, metrology and challenges. J Phys D: Appl Phys 2011;44(30):303001.
[4] Thomas L, Jan G, Zhu J, Liu H, Lee Y-J, Le S, et al. Perpendicular spin transfer torque magnetic random access memories with high spin torque efficiency and thermal stability for embedded applications. J Appl Phys 2014;115(17):172615.
[5] Xue L, Nistor L, Ahn J, Germain J, Ching C, Balseanu M, et al. A self-aligned two-step reactive ion etching process for nanopatterning magnetic tunnel junctions on 300 mm wafers. IEEE Trans Magn 2014;50(11):10–2.
[6] Cagliani A, Osterberg FW, Shiv L, Nielsen PF, Hansen O, Petersen DH. Breakthrough in current in plane metrology for monitoring large scale MRAM production; 2017. p. 1–3.
[7] Jeong J, Endoh T. Ion beam etching process for high-density spintronic devices and its damage recovery by the oxygen showering post-treatment process. Jpn J Appl Phys 2017;56(4S):04CE09.
[8] Dave RW, Steiner G, Slaughter J, Sun J, Craigo B, Pietambaram S, et al. MgO-based tunnel junction material for high-speed toggle magnetic random access memory. IEEE Trans Magn 2006;42(8):1935–9.
[9] Kim JH, Lim W, Pi U, Lee J, Kim W, Kim J, et al. Verification on the extreme scalability of STT-MRAM without loss of thermal stability below 15 nm MTJ cell. In: 2014 symposium on VLSI technology (VLSI-technology): digest of technical papers. 2014. p. 1–2.

[10] Leitao DC, Silva AV, Paz E, Ferreira R, Cardoso S, Freitas PP. Magnetoresistive nanosensors: controlling magnetism at the nanoscale. Nanotechnology 2016;27(4):045501.
[11] Chun SW, Kim D, Kwon J, Kim B, Choi S, Lee SB. Multi-step ion beam etching of sub-30 nm magnetic tunnel junctions for reducing leakage and MgO barrier damage. J Appl Phys 2012;111(2012):2010–3.
[12] Macedo R, Borme J, Ferreira R, Cardoso S, Freitas PP, Mendis B, et al. Nanofabrication of 30 nm devices incorporating low resistance magnetic tunnel junctions. J Nanosci Nanotechnol 2010;10:5951–7.
[13] Costa JD, Serrano-Guisan S, Borme J, Deepak FL, Tarequzzaman M, Paz E, et al. Impact of MgO thickness on the performance of spin-transfer torque nano-oscillators. IEEE Trans Magn 2015;51(11):1–4.
[14] Ding Y, Pakala M, Nguyen P, Meng H, Huai Y, Wang JP. Fabrication of current-induced magnetization switching devices using etch-back planarization process. J Appl Phys 2005;97(2005):2003–6.
[15] Knudde S, Leitao D, Cardoso S, Freitas P. Annealing free magnetic tunnel junction sensors. J Phys D: Appl Phys 2017;50(16):165001.
[16] Goodberlet JG, Hastings JT, Smith HI. Performance of the Raith 150 electron-beam lithography system. J Vac Sci Technol B 2001;19(September):2499.
[17] Silva AV, Leitao DC, Huo Z, Macedo RJ, Ferreira R, Paz E, et al. Switching field variation in MgO magnetic tunnel junction nanopillars: experimental results and micromagnetic simulations. IEEE Trans Magn 2013;49(7):4405–8.
[18] Gajek M, Nowak JJ, Sun JZ, Trouilloud PL, O'Sullivan EJ, Abraham DW, et al. Spin torque switching of 20 nm magnetic tunnel junctions with perpendicular anisotropy. Appl Phys Lett 2012;100:1–4.
[19] Wang W, Pearse A, Li M, Hageman S, Chen A, Zhu F, et al. Parallel fabrication of magnetic tunnel junction nanopillars by nanosphere lithography. Sci Rep 2013;3:1948.
[20] Jeon MH, Yang KC, Park JW, Yun DH, Kim KN, Yeom GY. Etch residue removal of CoFeB using CO/NH3 reactive ion beam for spin transfer torque-magnetic random access memory device. J Vac Sci Technol B 2015;33:061212.
[21] Kinoshita K, Honjo H, Fukami S, Sato H, Mizunuma K, Tokutome K. Process-induced damage and its recovery for a CoFeB – MgO magnetic tunnel junction with perpendicular magnetic easy axis. Jpn J Appl Phys 2014;53:103001.
[22] Sugiura K, Takahashi S, Amano M, Kajiyama T, Iwayama M, Asao Y, et al. Ion beam etching technology for high-density spin transfer torque magnetic random access memory. Jpn J Appl Phys 2009;48:48–51.
[23] Kinoshita K, Utsumi H, Suemitsu K, Hada H, Sugibayashi T. Etching magnetic tunnel junction with metal etchers. Jpn J Appl Phys 2010;49(08JB02).
[24] Peng X, Wakeham S, Morrone A, Axdal S, Feldbaum M, Hwu J, et al. Towards the sub-50 nm magnetic device definition: ion beam etching (IBE) vs plasma-based etching. Vacuum 2009;83(6):1007–13.
[25] Park JY, Kang SK, Jeon MH, Jhon MS, Yeom GY. Etching of CoFeB using CO/NH3 in an inductively coupled plasma etching system. J Electrochem Soc 2011;158(H1-H4).
[26] Greve MM. Optimization of an electron beam lithography instrument for fast, large area writing at 10 kV acceleration voltage. J Vac Sci Technol B 2013;31:043202.
[27] Scholten K, Meng E. Electron-beam lithography for polymer bioMEMS with submicron features. Micros Nanoeng 2016;2:16053.
[28] Dey RK, Cui B. Stitching error reduction in electron beam lithography with in-situ feedback using self-developing resist. J Vac Sci Technol B 2013;31:06F409.
[29] Leitao DC, Coelho P, Borme J, Knudde S, Cardoso S, Freitas PP. Ultra-compact $100 \times 100\,\mu m^2$ footprint hybrid device with spin-valve nanosensors. Sensors 2015;15(12):30311–8.
[30] Leitao DC, Silva V, Ferreira R, Paz E, Deepack FL, Cardoso S, et al. Linear nanometric tunnel junction sensors with exchange pinned sensing layer. J Appl Phys 2014;115:18–21.
[31] Bapna M, Piotrowski SK, Oberdick SD, Li M, Chien C-L, Majetich SA. Magnetostatic effects on switching in small magnetic tunnel junctions. Appl Phys Lett 2016;108(2):022406.
[32] Lv H, Leitao DC, Hou Z, Freitas PP, Cardoso S, Kampfe T, et al. Barrier breakdown mechanism in nano-scale perpendicular magnetic tunnel junctions with ultrathin MgO barrier. AIP Adv 2018;8(5):055908.